Displays 29 (2008) 506–511

Contents lists available at ScienceDirect

Displays

journal homepage: www.elsevier.com/locate/displa

LED brightness control for video display application

L. Svilainis *

Signal Processing Department, Kaunas University of Technology, Studentu Str. 50, TEF#340, LT-51368 Kaunas, Lithuania

ARTICLE INFO

Article history:
Received 21 June 2006
Received in revised form 22 April 2008
Accepted 13 May 2008
Available online 20 May 2008

Keywords:
LED dimming
LED video display
Pulse-width-modulation
LED display electronics

ABSTRACT

The technique is suggested for a kind of pulse-width-modulation LED dimming in LED video displays. The significant increase of the gray levels number and image refresh frequency can be achieved when the large number of LEDs is controlled serially. The need for a large number of grayscale levels and high refresh rate is explained. The controlling data flow and the amount of buffer memory are the same as with binary-weighted pulse-width-modulation. Spreading the switching pulses in time reduces the electromagnetic interference.

1. Introduction

Several decades had passed from the first Light emitting diode (LED) application for the imaging. The latest traced paper was dated before 1974 [1]. Nowadays LED displays are used in road and railway signage facilities, banks, stock exchanges, airports, advertising, etc. [2]. This device presents the superlative source of information and video image display with a wide viewing angle and a bright and clear image [3].

However, LED properties nonlinearly depend on diode forward current. Therefore, pulse-width-modulation (PWM) with the constant current is used to drive the LED. Then the light output regulation is linear. This is the major difference from such conventional imaging devices as cathode-ray-tube (CRT). Due to nonlinearity of human sense of light, LED display pixel brightness coding require the higher levels' number since some codes have to be removed to create the desired control law. Another difference from CRT is that every LED has to have the individual power supply. In CRT this is accomplished by electron beam hitting the screen points sequentially. The serial data transmission reduces the number of control signals. The necessity transmission limits the shortest obtainable light pulse width. The LED display image refresh frequency has to be kept to a certain level. These will restrict the number of attainable LED intensity levels.

The intention of this paper is to present a LED dimming method suitable for the overcoming of the mentioned limitations.

2. Problem description

Human vision or rather human brain needs to be deceived by the imaging device. Therefore the display performance should somehow simulate the human response. This has to be taken into account in LED dimming for video display applications. The LED light is produced by the phenomenon of luminescence [4]. The LED needs to be driven by a DC current source in order to generate the illumination. The forward current affects the LED emission wavelength, especially for InGaN, which today is favored for the highest brightness. The LED operation at constant current would ensure the screen color gamut stability. In such a case, the PWM can replace the LED light output intensity control by the current [5].

2.1. The linear PWM for LED brightness control

The average power of PWM is linearly proportional to the pulse duration. This offers a convenient and simple LED intensity control mechanism [6,7]. Taking the 100% duty luminance as Y_n, any other duty cycle will give luminance level Y proportional to pulse duration τ ratio to PWM period T

$$Y = Y_n \frac{\tau}{T}. \tag{1}$$

This level's stability and repeatability is easily established since frequency stability can be easily achieved using quartz oscillators. Only the amount of available duration steps limits the number of dimming steps. Refer to Fig. 1 for linear PWM explanation.

The linear PWM has one inherent disadvantage: no matter what the pixels intensities are there will be a moment (position 1 in Fig. 1) when all the LEDs are switched on. A large current spike will oc-

* Corresponding author. Tel.: +370 37 300532; fax: +370 37 352998.
E-mail addresses: svilnis@ktu.lt.

0141-9382/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.displa.2008.05.002

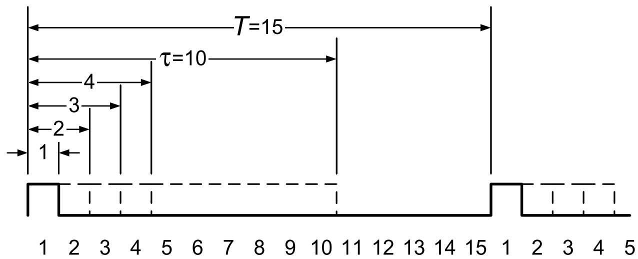

Fig. 1. The explanation of linear PWM operation.

cur on power supply line at this time instant, causing an EMI problem.

2.2. Binary-weighted PWM

The binary-weighted PWM (BPWM), the discrete PWM [7] or bit angle modulation (BAM) [8] dimming use different weight for the pulses in a period to form the required duty. This type of dimming will reduce EMI by spreading a current surge spikes in time. Refer to Fig. 2 for the conventional and weighted PWM comparison.

The width of each separate pulse is proportional to the weight of the bit in the corresponding binary code. But the summary pulse width is the same as conventional PWM. The BPWM driving simplifies the system design and reduces the amount of required memory.

2.3. Multiple LED control

The majority of display designs use a serial LED control [6,9]; every display controller should control as much as possible LEDs [9] in order to reduce the control electronics complexity and the price. Data are serially shifted out of controller in order to reach the LED. Serial data delivery will reduce the amount of control wires. Refer to Fig. 3 for general driver topology drawing.

Such approach is used both for the multiplex (dynamic) [6] and the direct (static) [10] drive techniques. The data shifting process should not be visible on-screen therefore driver usually contains two storage levels [10–14]. The first layer is the shift register, responsible for serial data reception. It contains a serial data input (SDI) node, shift register data output (SDO) for cascading and a clock signal (CLK) terminal. The last level is the latch, responsible for holding the previous data. Latching from the shift register to the upper layer latch is controlled by the separate control line (LTD). An output stage is using the data from the last layer latch for the LED control. The most popular constant output current driver topology is presented in Fig. 4.

The constant current sink is provided by individual regulated current sources. Single external resistor sets this sink current.

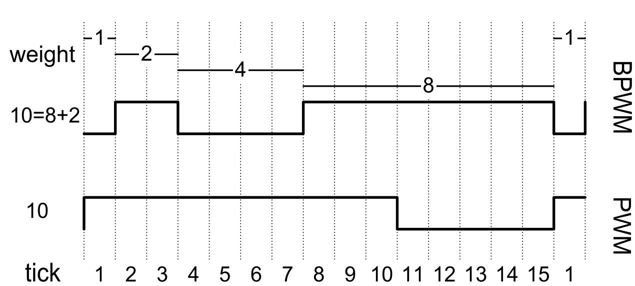

Fig. 2. Binary-weighted PWM and conventional PWM comparison for the same level.

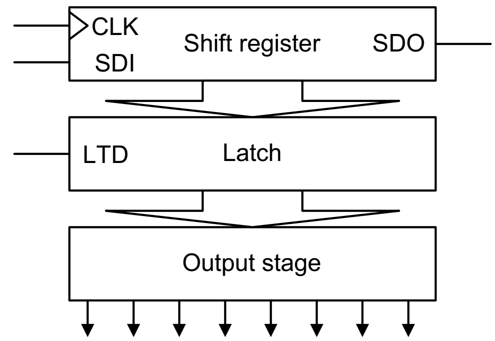

Fig. 3. General LED driver topology.

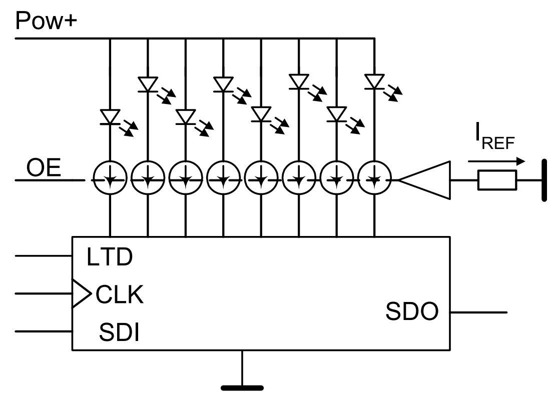

Fig. 4. Constant current output driver topology.

The current source is turned on when a logical “1” is stored in the upper layer latch. The current source is turned off (high output impedance state) if latch contains logical “0”. All current sinks can be directly turned-off using an output enable (OE) signal.

Table 1 summarizes several constant current topology LED drivers presented in the market [10–14]. The maximal output current match is specified for the channels on the same IC and between ICs. The OE signal propagation time t_{PHL} and t_{PLH} are important for the scope of this paper. The shortest OE signal duration should not get below the sum of t_{PHL} and t_{PLH}.

The following conclusions can be drawn from this chapter:

- data are delivered to the LED drivers using shift registers;
- clock speed is limited by technology and currently is about 25 MHz;
- almost all the drivers have OE signal;
- driver speed allows approximately 200 ns duration of driving signal.

2.4. Gamma correction

Scene lightness sensation L^* of human vision is nonlinear [15]. It is roughly a power function of luminance Y. CIE publication [16] recommends the following approximation

$$L^* = \begin{cases} 116(\frac{Y}{Y_n})^{\frac{1}{3}} - 16, & \frac{Y}{Y_n} > 0.008856 \\ 903.3\frac{Y}{Y_n}, & \frac{Y}{Y_n} < 0.008856 \end{cases}, \tag{2}$$

where Y_n is the luminance of the white reference. The camera used for the image capturing simulates the human visual system in order to sense the lightness in the same way as a human spectator would. Coding of the incoming image intensity into a γ-corrected signal makes maximum perceptual use of the channel. The nonlinear signal is transformed back to the linear intensity at the display using

Table 1
The drivers with constant current output

Part	I_{OUT}max, mA	I_{OUT}match, % ch/% IC	f_{CLK}max, MHz	t_{PHL}, ns	t_{PLH}, ns
A6279	90	6/–	25	75	75
DM135B	60	4/6	25	20	30
TB62727	60	4/12	20	140	170
MBI5168	120	3/6	25	100	100
STP16C596	120	4/10	25	45	145
MAX6969	55	3/6	25	100	320

the nonlinear voltage-to-intensity response inherent for the CRT. The luminance Y of the CRT is approximately equal to the applied voltage U raised to the 2.3–2.6 power. The numerical value of the exponent of this power function is known as "gamma" and is marked by Greek γ giving the name for correction function. In the simplest form it can be written

$$Y = U'^{\gamma}, \tag{3}$$

where Y is the RGB tristimulus value of R, G or B with the prime index denoting the signal voltage or code and index-free is the CRT light intensity.

The CRT voltage-to-intensity response is approximately the inverse of the luminance-to-lightness relationship of vision. Therefore only minor correction is needed when the image is displayed on CRT. The artificial γ correction is obligatory when the image is displayed on linear response display (e.g. PWM dimming).

2.5. The amount of PWM bits for gamma correction

Mathematically the pixel code C_{in} conversion to inverse-gamma corrected code C_γ with resolution of N bits can be expressed as

$$C_\gamma = \mathrm{round}\left(\left(\frac{C_{in}}{2}55\right)^{\gamma} 2^N\right) \tag{4}$$

The diagrams presenting the result of such conversion for 8, 10, 12, 14, 16, and 19 bits resolution and 2.5 gamma correction are presented in Fig. 5.

The diagram (Fig. 5) shows that the only code using 19 bit resolution is capable of monotonic variance: every increment of the input code is causing the increment of the output code. Such gamma correction will exhibit some approximation error even with the high resolution output code

$$\delta_{approx} = \frac{\left(C_{CRT} - \left(\frac{C_{in}}{255}\right)^{\gamma} 2^N\right)}{\left(\frac{C_{in}}{2}55\right)^{\gamma} 2^N} \cdot 100\% = \left(\frac{C_{CRT}}{\left(\frac{C_{in}}{255}\right)^{\gamma} 2^N} - 1\right) \cdot 100\%. \tag{5}$$

The approximation error will be large at the lower end of the input codes: this can be clearly seen at graphical error presentation in Fig. 6.

Analysis of the error distribution over the input code range and the output code resolution can be summarized in Table 2. The minimum code numbers ensuring the approximation error of gamma corrected output is below the specified limit are listed.

Gray scale could be referred as the number of luminance levels (shades of gray), available at a display. The reference [17] indicates that human eye can discriminate the luminance ratio between the levels as small as 1.03. It could be understood that luminance difference between two patches by more than 3% can be detected. Only PWM codes above 34 can satisfy this requirement. Fortunately, common definition is a luminance ratio of 1.4 between levels [17]. Then the PWM codes above three will satisfy the requirement. For gamma corrected output this will correspond to input code 46 for 8 bit, 28 for 10 bits, 17 for 12 bits, 9 for 14 bits, 5 for 16 bits, and 4 for 19-bit gamma correction coding. Table 1 indicates that LED driver current mismatch can reach 6%. This means that the expected luminance level will be distorted by LED driver. Therefore it makes no sense in reaching gamma correction curve match better than that; this will correspond to 5% in Table 2. Then the best alternative seems to be 14 bit coding since there is no sense in using 16 or 19 bit gamma correction coding.

2.6. The flicker

The flicker occurs when the changes in the display luminance occur at the frequency below the integrating capability of the

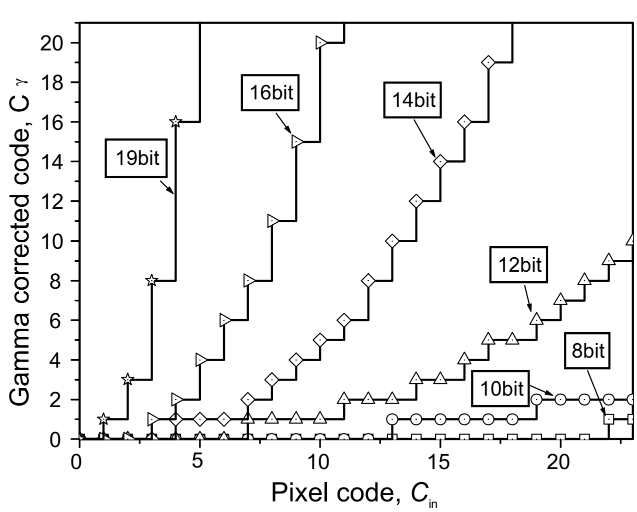

Fig. 5. Gamma correction codes for various bit resolutions.

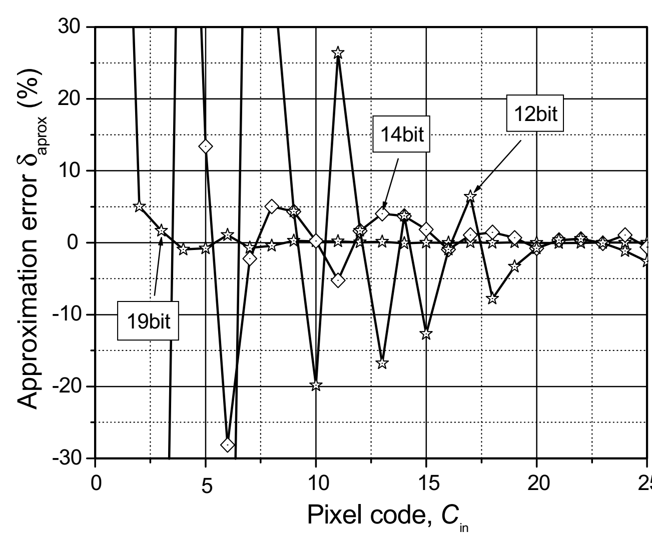

Fig. 6. Gamma correction approximation error.

Table 2
Minimum input codes with approximation error below specified limit

Err, %	8 bit	10 bit	12 bit	14 bit	16 bit	19 bit
10	47	30	16	7	6	2
5	63	35	19	12	7	2
2	94	51	31	15	10	3
1	122	69	42	25	14	7

eye. The minimum frequency at which this occurs is the critical flicker fusion frequency (CFF) [17]

$$\mathrm{CCF} = a \log L_a + b, \tag{6}$$

where $a = 12.5$ (for high ambient light level) or 1.5 (for low ambient light level), L_a is the average luminance of the image in cd/m^2, or nits, and $b = 37$. An 87 Hz CFF is obtained taking the LED screen luminance 10,000 cd/m^2 as high and assuming a high ambient light level. In practice the image refresh frequencies can reach 100 Hz. In the professional LED screen application, not a human vision is the factor determining the image refresh frequency. The reason is that usually almost every event is captured on camera for clip production or TV broadcasting. The camera sensitivity can be controlled by adjusting the aperture size when the scene background is relatively dim. When the scene becomes very bright, the aperture size reduction is not sufficient and the camera exposure time has to be varied. In case the LED screen refresh is slower compared to camera exposure time, then only part of the PWM dimming cycle is captured. This will create the image distortion. Synchronization to video equipment frequency is not sufficient. Therefore the refresh rate needs to be much higher than the requirement for human spectator. Usually 1000–400 Hz refresh frequency is used. Some manufacturers claim success at 240 Hz refresh [18].

2.7. Problem rectification

Both linear and binary-weighted PWM refresh cycles can be subdivided into sub-frames (ticks). This sub-frame data (“1” or “0”) has to be delivered to every LED driver channel. This data are supplied by shifting serial data through driver registers. The sub-frame loading time τ_{load} required to shift-load N_{REG} channels of LED driver at shifting clock frequency f_{CLK} can be calculated as

$$\tau_{\mathrm{load}} = \frac{1}{f_{\mathrm{CLK}}} \times N_{\mathrm{REG}}. \tag{7}$$

This time is limiting the minimum attainable duration of PWM signal. For instance, the shortest duration will be 1280 ns, for 32 channel LED driver, for 96 LED it will be 3840 ns, etc. The required refresh frequency f_{refr} defines the PWM period duration T_{refr} which in turn defines the number of available levels

$$n_{\mathrm{PWM}} = \frac{T_{\mathrm{refr}}}{\tau_{\mathrm{load}}}. \tag{8}$$

The data in Table 3 list the available levels n_{PWM} and corresponding bits numbers versus driven LED number and versus refresh frequency used for the few specific cases of LED drive. Note that the amount of available levels n_{PWM} has been converted into N_{b} bits. The bit numbers were rounded. This corresponds that the refresh frequency has to be lowered while rounding up and increased if rounding down. The limit for decrease will be 75% and 150% for increase. Otherwise, if frequency decrease is unwanted, 1 bit of available coding has to be sacrificed. In the case of the linear PWM, the sub-frames number will be equal to the number of PWM steps. The sub-frames number for the binary PWM is defined by binary bits number. This means that much less data have to be sent in the case of BPWM. The 2^N levels are obtained by 2^N load operations in the case of PWM with N bits. Compare this to N loads to obtain the same 2^N levels in the case of BPWM. Therefore BPWM technique seems to be more attractive for LED video

Table 3
PWM levels number/bits available for 25 MHz serial data clock

Refresh, Hz	Levels number/bits				
	50	100	240	400	1000
LEDs					
1	500000/19	250000/18	104167/17	62500/16	25000/15
8	62500/16	31250/15	13021/14	7813/13	3125/12
16	31250/15	15625/14	6510/13	3906/12	1563/11
32	15625/14	7813/13	3255/12	1953/11	781/10
96	5208/12	2604/11	1085/10	651/9	260/8
256	1953/11	977/10	407/9	244/8	98/7

display control, especially keeping in mind that the incoming video data usually comes in the binary format.

It should be noted that the numbers obtained for one LED are not applicable. Table 3 indicates that the shortest PWM pulse duration is 40 ns if shift frequency is 25 MHz. But the available LED switching speed and the required refresh frequency limit the number of available steps for any type of PWM. The manufacturers do not specify LED response time. The study carried out at [19,20] indicated that LED response time is slightly below 100 ns. Table 3 data analysis indicates that increasing the number of LEDs to be driven serially will significantly degrade the display performance. The reasonable number (256) of LEDs used for serial control will not allow more than 10 bits for the refresh rate above 100 Hz.

3. Solution: gated PWM

Since the main limitation on the shortest light pulse is the data loading time, so the additional gating of the LED lighting is suggested. Such improved PWM makes use of the fact that the OE signal duration can be much shorter than the duration required for loading the entire sub-frame data. The LED is lit-on only for a short duration $\tau_{\min}$ (Fig. 7) during the data loading operation instead of the shortest PWM duration defined by the frame data load time τ_{load}. This will correspond to replacing the τ_{load} used Eq. (8) to $\tau_{\min}$. In such a way almost unlimited number of PWM levels can be achieved. Despite this technique can be applied for linear PWM, most of the performance gain is achieved when in combination with the binary-weighted PWM. The suggested technique is named as Gated PWM (GPWM).

The sub-frame (tick) length used in Fig. 7 is the same as used in Fig. 2. The comparison of figures indicates that not only the refresh period has been reduced (from 15 to 10) but also the levels number has been increased (from 15 to 63).

4. GPWM performance

There are two factors limiting the performance of the blanking. Both are related to the shortest achievable LED flash duration,

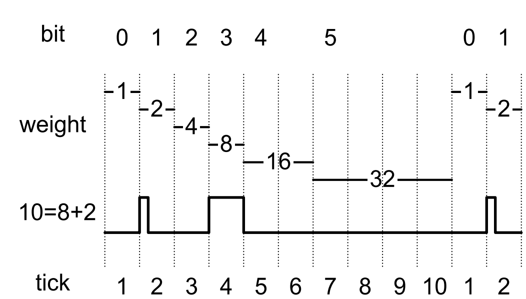

Fig. 7. The additional gating of GPWM.

where one is the LED driver's response. The other limiting factor is the LED response time. As noted in Table 2, the best propagation delay for high and low level is 100 ns. Then 200 ns should be used as minimal GPWM duration $\tau_{\min}$. Study [20] indicated that LEDs commonly used for video screens have response time below 100 ns. Refer to Fig. 8 for the explanation of the attainable levels calculation.

The desired refresh frequency f_{refr} defines the period duration T_{refr}. The amount of available levels n_{G} because of gating introduction is:

$$n_{\mathrm{G}} = \frac{\tau_{\mathrm{load}}}{\tau_{\min}}. \tag{9}$$

The remaining levels number n_{M} is the number of levels that would be attainable if PWM or BPWM techniques are used:

$$n_{\mathrm{M}} = \frac{T_{\mathrm{refr}} - N_{\mathrm{G}} \cdot \tau_{\mathrm{load}}}{\tau_{\mathrm{load}}}. \tag{10}$$

The total available bits are the sum of n_{G} and n_{M}. This will correspond to the number of bits

$$N_{\mathrm{tot}} = \log_2(n_{\mathrm{G}} + n_{\mathrm{m}}). \tag{11}$$

The data presented in Table 4 list the GPWM bits obtained. The minimal duration of 200 ns was used. The serial data clock is the same as used in Table 3.

Note the GPWM performance improvement over conventional PWM (Table 3). The number for achievable refresh frequency and levels number for conventional PWM largely depend on the amount of the controlled LEDs. There is a significant reduction of the influence of the amount of controlled LEDs on refresh frequency and levels number. For instance, the serial control of 256 LEDs refreshes only at 100 Hz and only 10 bits (977 levels) can be achieved for the conventional PWM (as well as BPWM). The GPWM technique can attain 16 bits (65536 levels) or 64 times more for the same conditions.

The other advantage of GPWM is explained in Fig. 9. As in the case of PWM, the number of bits listed in a Table 4 has been obtained by rounding the levels number. In the case of conventional PWM this means that refresh frequency has to be lowered if rounded up or increased, if rounded down. The same approach can be used with GPWM (refer to $T_{\mathrm{ref\ Rounded}}$ in Fig. 9), but GPWM also the other option is available. The most significant portion of the PWM cycle end is removed, but the additional, least significant, portion is added in front. It is interesting to note that refresh frequency now has to be increased, which is beneficial for image quality. Of course, this is at the expense of use of the shortest pulse of duration twice shorter than the one determined by LED reaction time (option A), or, shift clock frequency can be reduced (option B). Then pulse duration violation is not so immense.

The GPWM time diagrams on Fig. 9 indicate the slight disadvantage of the additional gating: the maximum available LED brightness is reduced. This is because of a period of time with deliberately switched off LED. The percentage of this time from total refresh period define the light output efficiency Eff_{GPWM}

$$Eff_{\mathrm{GPWM}} = 100\% - \frac{(N_{\mathrm{G}} - 1) + \frac{1}{2^{N_{\mathrm{G}}}}}{\frac{2^{N_{\mathrm{G}}+N_{\mathrm{M}}}}{2^{N_{\mathrm{G}}}} + N_{\mathrm{G}}} \cdot 100\%. \tag{12}$$

Table 5 summarizes the Eq. (12) results for 25 MHz serial data clock.

The loss of brightness above 10% can be considered as sufficient. But the highest loss indicated in Table 5 is close to 5%. The conclusion that loss in brightness is insufficient can be drawn.

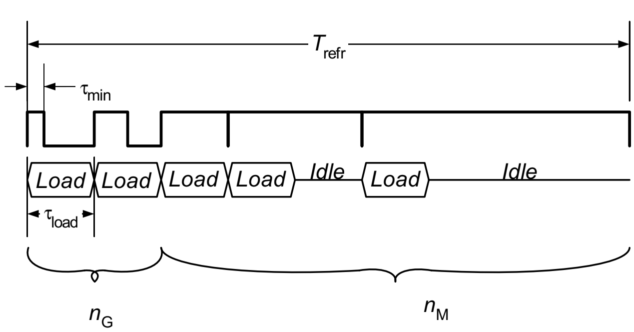

Fig. 8. The number of GPWM levels.

Table 4
GPWM bits available for 25 MHz serial data clock

Refresh, Hz	Bits				
	50	100	240	400	1000
LEDs					
1	17	16	14	14	12
8	17	16	14	14	12
16	17	16	14	14	12
32	17	16	14	14	12
96	17	16	14	14	12
256	17	16	14	14	12

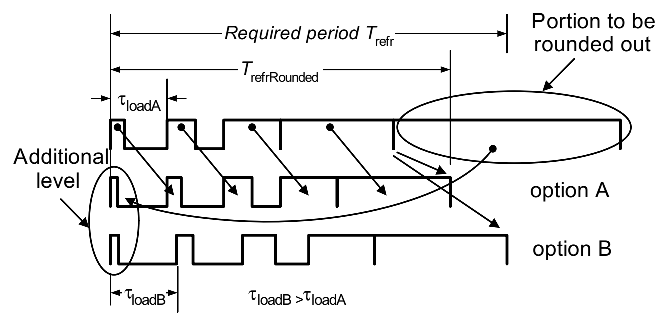

Fig. 9. Rounding options for GPWM.

5. Conclusions

The GPWM LED dimming technique is suggested for LED video displays where the large number of grayscale levels is needed. The technique is applicable when serial transmission of LED drivers' data is used. It is offering a significant increase of gray levels compared to PWM and BPWM. There is an insignificant decrease in the total light output. For the worst case analyzed the reduction in maximum achievable intensity is about 5% if 256 LED are driven serially and 1 kHz refresh frequency is used. GPWM maintains the advantages of the binary PWM: the controlling data flow and the amount of buffer memory used for the processing and storage is low. The switching pulses are spread in time so produce less EMI than the linear PWM.

Table 5
GPWM light output efficiency (%)

Refresh, Hz	Bits				
	50	100	240	400	1000
LEDs					
1	100	100	100	100	100
8	100	100	100	100	100
16	100	100	100	100	99.9
32	100	100	99.9	99.9	99.7
96	100	99.9	99.6	99.6	98.5
256	99.8	99.6	98.6	98.6	94.5

Acknowledgment

The author thank Dr. V. Dumbrava for a helpful discussions and critical notes.

References

[1] R. Haitz, Trends in LED display technology, machine design, in: Proceedings of 24th Electron Components Conference, 1974, pp. 2–10..
[2] V.S. Abramov, A.E. Puisha, I.P. Polyakova, M.G. Tomilin, A.I. Chuvashov, LED modules for large screens, Journal of Optical Technology (Opticheskii Zhurnal) 70 (2003) 492–494.
[3] F. Nguyen, Challenges in the design of a RGB LED display for indoor applications, Synthetic Metals 122 (2001) 215–219.
[4] E.F. Schubert, Light-Emitting Diodes, Cambridge University Press, 2003.
[5] P. Narra, Narra, D.S. Zinger Kurdthongmee, Design and implementation of an FPGA-based multiple-colour LED display board, Microprocessors and Microsystems 29 (2005) 327–336.
[7] M. Xichao, Xichao, Z. Yuanyue Gillessen, C. Malinowski, A.J. Marshall, W. Schairer, Survey of interconnection methods which reduce the number of external connections for LED displays, SID International Symposium 22 (1980) 181–184.
[10] MBI5168, 8-bit Constant Current LED Sink Driver, Datasheet VA02, Macroblock Inc., Taiwan, 2005.
[11] TB62727FN, 16-bit Constant Current LED Module with Built-in Dot-Current Correction for each Output, Toshiba Corporation, Japan, 2005.
[12] A6278 and A6279, Serial-Input Constant-Current Latched LED Drivers with Open LED Detection 6278-DS, Rev. 2, Allegro MicroSystems Inc., USA, 2006.
[13] MAX6969, 16-Port, 5.5V Constant-Current LED Driver 19-3677; Rev 1; 8/05, Maxim Integrated Products, CA, USA, 2005.
[14] STP16C596, 16-Bit, Constant Current LED Sink Driver, Ref. 5, ST Microelectronics, 2004.
[15] C.A. Poynton, Gamma and its disguises, Journal of the Society of Motion Picture and Television Engineers 102 (1993) 1099–1108.
[16] Recommendation ITU-R BT.709, Basic Parameter Values for the HDTV Standard for the Studio and for International Programme Exchange, Geneva: ITU 1990.
[17] S.A. Murray, Human factors in displays, in: Steven A. Murray, Barrett S. Caldwell (Eds.), Measurement Instrumentation and Sensors Handbook, CRC Press, LLC, 2000.
[18] B. Wendler, Refresh Rate, Technical Note , 42, Daktronics Inc., USA, 2002.
[19] A.B. Brailovsky, V.V. Mitin, Fast switching of light-emitting diodes, Solid-State Electronics 44 (2000) 713–718.
[20] L. Svilainis, LED PWM dimming linearity investigation, Displays 29 (2008) 243–249.