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Reliability of TSV interconnects: Electromigration, thermal cycling, and impact on above metal level dielectric

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ABSTRACT

In this paper, reliability of Through Silicon via (TSV) interconnects is analyzed for two technologies. First part presents an exhaustive analysis of Cu TSV-last approach of 2 μm diameter and 15 μm of depth. Thermal cycling and electromigration stresses are performed on dedicated devices. Thermal cycling is revealed to induce only defects on non-mature processes. Electromigration induces voids in adjacent metal level, right at TSV interface. Moreover, the expected lifetime benefit by increasing line thickness does not occur due to increasing dispersion of voiding mechanism. Second part covers reliability of Cu TSV-middle technology, of 10 μm diameter and 80 μm depth, with thermal cycling, BEoL dielectric breakdown, and electromigration study. Thermal cycling is assessed on two designs: isolated and dense TSV patterns. Dielectric breakdown tests underline an impact of TSV on the reliability of metal level dielectrics right above TSV. Electromigration reveal similar degradation mechanism and kinetic as on TSV-last approach.

1. Introduction

3D integration based on Through Silicon Via (TSV) is becoming an attractive alternative to overcome obstacles of CMOS scaling. The vertical stack of dice, using chip-to-chip interconnects and TSV, enables higher bandwidths and smaller footprints.

TSV technologies for mainstream integration schemes, such as Wide IO memory stacking [1–3] or TSV based passive interposers, appear today to crystallize around 5–10 μm diameter Cu TSV in 50–100 μm thick silicon. Whatever the presence of active devices in the Si strata having TSVs, first reliability concerns are located at interfaces of TSV and at adjacent metallization levels. And since TSV processes reach today maturity, reliability investigations become critical.

Early reliability studies of TSV based integrations started during the last decades with thermo-mechanical simulations, since the thermal expansion mismatch between Cu TSV and Si die is very large: Si and Cu Coefficient of Thermal Expansion (CTE) are respectively of about $3 \times 10^{-6}\,°C^{-1}$ and $17 \times 10^{-6}\,°C^{-1}$. Several studies evaluated, through simulations, fatigue of Cu TSV, delamination at TSV interfaces, and Si cracking due to thermo-mechanical stress. These studies point out that the existence of the copper through-vias affects the stress distributions and the interconnection reliability [4–9]. Maximum computed stresses, and related expected failures in the TSV, are localized at interfaces to adjacent metal levels [4,6]. Consequently, early experimental reliability studies of TSV, focused on Thermal Cycling (TC) assessments [10–12]. However, authors underlined the overall robustness of TSV interconnects.

Besides TC, mainly three other failure mechanisms have been recently started to be studied for TSV based integrations: Electromigration (EM) induced voiding due to matter flux divergence at TSV interfaces [13–17]; impact of TSV on adjacent Back End of Line (BEoL) dielectrics reliability [18,19]; and Cu diffusion from TSV into active silicon [20,21]. Regarding EM, most studies focus on matter flux diffusion modeling at TSV interfaces [13–15]. However, these models lack of metallization barrier (like TaN or TiN) between the TSV and the adjacent metal levels. These barriers, today integrated in all the main-stream TSV interconnects, are a key item regarding the matter flux divergence due to electromigration.

In this paper, concerns of TC, EM, and impact of TSV on adjacent BEoL dielectric reliability, are addressed following two parts. First part presents an exhaustive experimental analysis of a high density Cu TSV-last technology of 2–4 μm diameters, and 15 μm of depth: TC and EM stresses are performed on dedicated devices focusing at TSV interfaces. Second part covers experimental reliability of Cu TSV-middle technology of 10 μm diameter and 80 μm thickness. TC, impact of TSV on BEoL dielectric breakdown, and EM degradation are addressed.

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Note that the key difference between the concepts of TSV-last and TSV-middle, is related to the process sequences: TSV-last, stands for integrations for which TSV is processed after the BEoL interconnects. For TSV-middle, the TSV is processed after Front End of Line (FEoL) and before BEoL. Although this difference is critical regarding thermal budgets of processes, the reliability issues are comparable, since related TSV interfaces are similar for both TSV-last and TSV-middle approaches.

2. Reliability of high density Cu TSV-last

2.1. Process description

A test vehicle has been designed and fabricated to analyze process, electrical performances and reliability of a high density Cu TSV-last technology, with diameters in the range of 2–5 μm, processed in a 15 μm thick Si strata. First process and electrical performances have been addressed in previous papers [22,23]. Concerning reliability, the test vehicle contains structures dedicated to address mainly TC and EM stresses. Since no chip-to-chip interconnects, i.e. solder bumps, are required to monitor the structures, the test vehicle enables a direct access to intrinsic reliability of TSV interconnects.

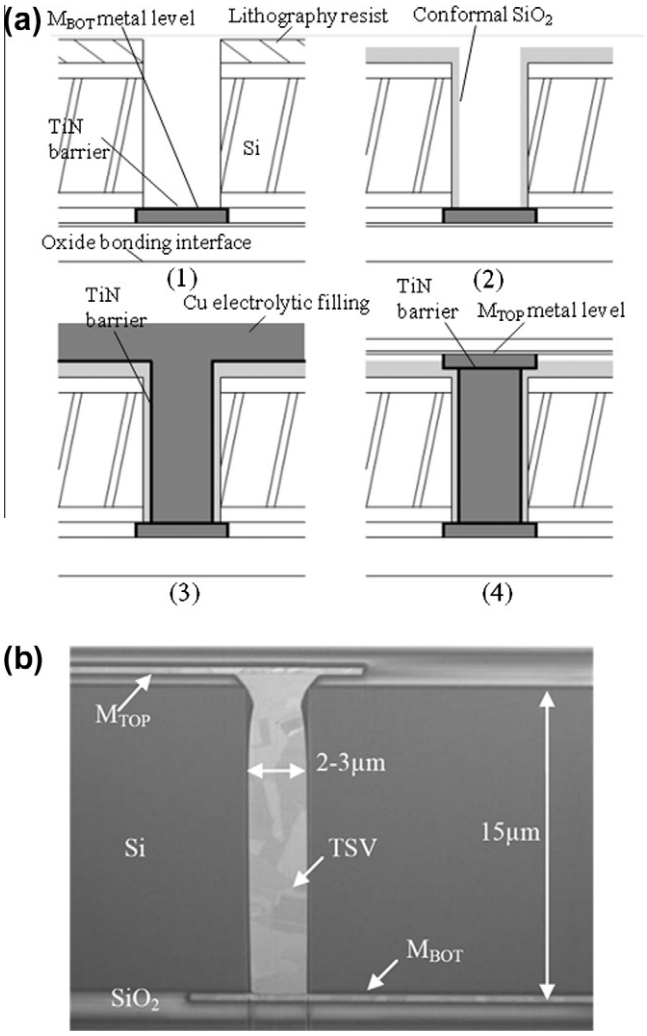

Fig. 1. (a) Schematic description of the TSV-last process steps: (1) Deep Reactive Ion Etching (DRIE). (2) Isolation with conformal SiO_2 and bottom opening with etch-back. (3) TiN barrier deposition, Cu seed and electrolytic filling. (4) Annealing, CMP, and Cu damascene redistribution level (M_{TOP}) and (b) SEM cross section of Cu TSVlast.

The technology is based on a stack of two silicon wafers using Direct Bonding technology [22]. A 200 mm wafer with one Cu damascene level (M_{BOT}) is bonded face down on a Si bulk carrier using SiO_2 bonding, and thinned down to 15 μm. The main steps of the high density Cu TSV-last process are depicted in Fig. 1a: (1) Deep Reactive Ion Etching (DRIE) to etch dielectric and silicon layers; (2) insulation with conformal SiO_2 and bottom opening with etch-back; (3) TiN barrier deposition, Cu seed and electrolytic filling; (4) annealing, CMP, and Cu damascene redistribution level (M_{TOP}). Both Cu metal levels have a TiN encapsulation barrier, and a SiN capping, and since M_{BOT} is processed prior to wafer bonding, both M_{BOT}/TSV and M_{TOP}/TSV interfaces are TiN (Fig. 2). Note that the SiO_2 isolation opening at the TSV bottom by etch-back, during the process step (2), induces a difference of interfacial size between the top and the bottom of the TSV. Bottom and top widths are respectively of 2.3 and 3.4 μm (Fig. 2).

2.2. Thermal Cycling

In this section, Thermal Cycling (TC) is performed on 2.3 μm and 4.2 μm TSVs for two processes: a non-mature A-process, and an optimized B-process. A Kelvin TSV structure is monitored before and after thermal cycling. It enables a usual four point sensing of the pure TSV resistance, based on separates pairs of voltage and current leads. Initial electrical characterizations of A-process reveal that for both diameters, the distributions of Kelvin TSV resistance values are multimodal (Fig. 3). Following their slope, distributions are divided into core and extrinsic populations. Breakpoints of distributions are for 2.3 μm and 4.2 μm diameters respectively at 19 mΩ and 70 mΩ. The lowest branch of the distributions with values under 19 mΩ/70 mΩ, corresponds to samples within the core process. The highest branch counts for samples having resistance values even one to two order magnitudes higher than core samples, and therefore considered as extrinsic, since out of core electrical specifications.

Physical analyses, based on Energy-Filtering TEM (EFTEM), and Scanning TEM (STEM) analysis (Fig. 4) at bottom of TSV, highlight an impurity layer containing carbon for only extrinsic samples. This impurity layer is assumed to result from a polymerization reaction of fluorocarbon plasma [24] used for reactive pre-cleaning after the etch-back of the TSV bottom. It reduces significantly the conduction surface leading to the higher electrical resistance for extrinsic samples. Regarding the cumulative level of slope breaks, 38% and 64% for respectively 2.3 μm and 4.2 μm (Fig. 3), the smaller diameter TSV is more impacted. The optimized B-process, including an enhanced pre-cleaning step after TSV etch-back, enables extrinsic free populations of resistance values (Fig. 3).

TC test, consisting of 500 cycles between −65 °C and +150 °C with 2 cycles per hour according to JEDEC standard [25], is performed on Kelvin TSVs of both processes. Resistance changes plots (Fig. 5) after TC underline that for A-process, the resistance change is much higher for extrinsic populations than for core populations. Concerning B-process, no shift above 10 % is observed, underlining, that the longer reactive pre-cleaning, avoids initial extrinsic populations, and ensures to pass TC assessments.

2.3. Electromigration

Maximal direct current rules for designers are given by the ageing of interconnects under electromigration (EM) phenomenon, which is the movement of metal atoms, in response to electron flux. At interfaces of atoms flux divergences, EM leads to voids and therefore to open circuit failure. Recent papers studied EM concerns at TSV interfaces, through simulation [13–15], and also

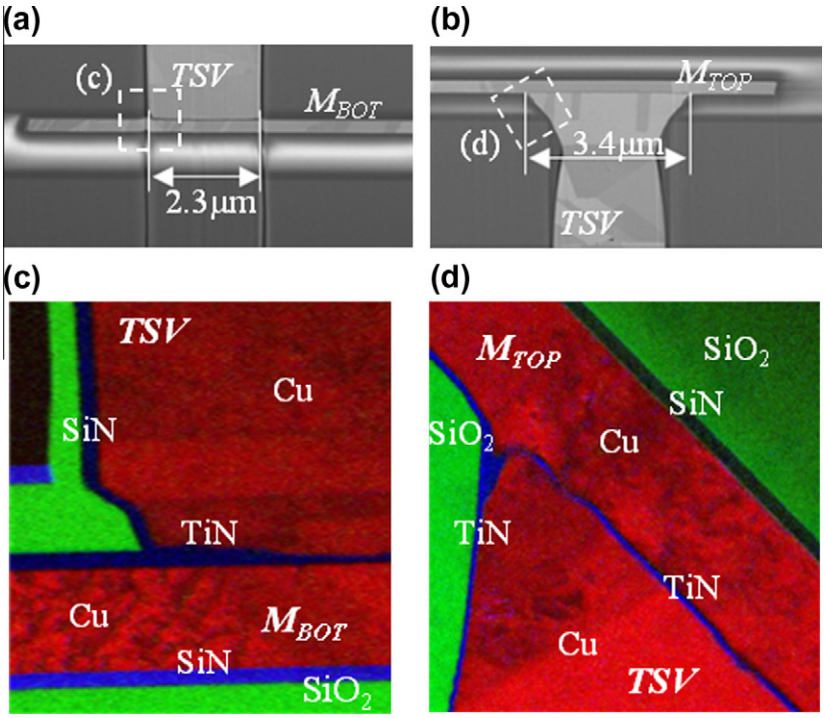

Fig. 2. (a and b) SEM cross section views of TSV bottom and top interfaces, with dotted boxes for the respective TEM mappings. (c and d) TEM chemical mapping of the interfaces.

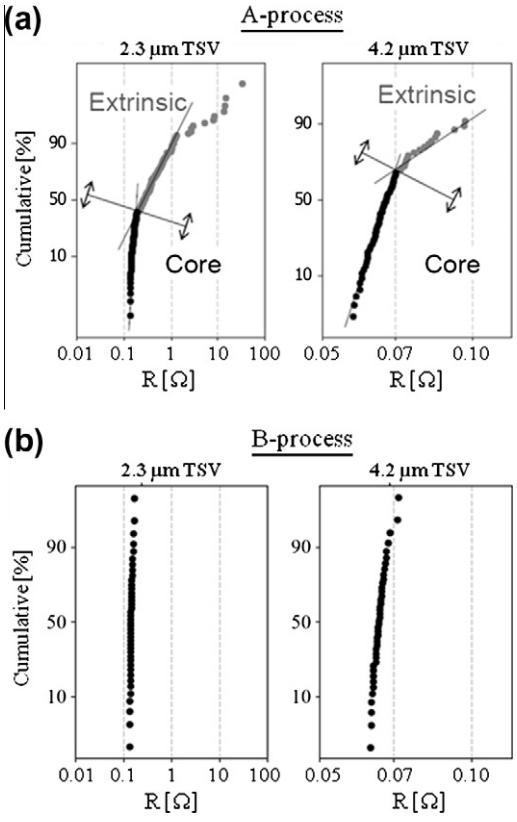

Fig. 3. Log-normal plots of initial resistance: (a) 2.3 µm diameter TSV and 4.2 µm diameter TSV of A-process and (b) 2.3 µm diameter TSV and 4.2 µm diameter TSV of B-process.

through first experimental approaches [16–17]. Concerning 3D integration based on high density TSV, with diameters below to 10 µm [19,26–27], TSV has two critical interfaces regarding EM: (1) transition between TSV and first metal level of Back End of Line (BEoL) – which is a thin metallization having a thickness below 0.25 µm and (2) transition between TSV and backside redistribution level – a thick metallization of about 1–5 µm.

This part of the paper studies the impact of TSV section size at the interface with adjacent metallization on EM lifetime by comparing up- and down-stream configurations since top and bottom of TSV have different diameters as (Fig. 6). Moreover, two Cu damascene processes are tested: thin metal level of 250 nm and thick metal level of 3.0 µm. EM tests are performed at package level.

Note that previously mentioned impurity layer, inducing extrinsic TSV populations, is found to have no visible impact on EM Time To Failure (TTF) and is therefore not discussed in this section.

2.3.1. Experimental

For the thin metal process, stress currents and temperatures are respectively of 15/25 mA, and 270/300 °C. For the thick metal process, stress currents and temperatures are respectively of 60/180 mA, and 270/300 °C. Stress conditions are detailed in Table 1. Initial measurements by computing Temperature Coefficient of Resistance (TCR), evaluate Joule heating to be below 5 °C.

Electrical resistance is monitored through four-point sensing during EM test. Resistance traces during EM tests have a first latency period where the resistance remains constant followed by an increase (Fig. 7).

2.3.2. Failure analyses

Reconstructed pictures from a 3D FIB–SEM (Focus Ion Beam–Scanning Electron Microscopy) analysis made on a down-stream configuration of thin metal before and after resistance increased, reveal that void nucleates in M_{BOT} inside the perimeter of the TSV bottom section (Fig. 8). We assume that the zone of maximal tensile stress leading to the void nucleation is right under the TSV, since the migration of incoming Cu atoms in this zone is blocked due to the TiN diffusion barrier whereas the atoms leaving

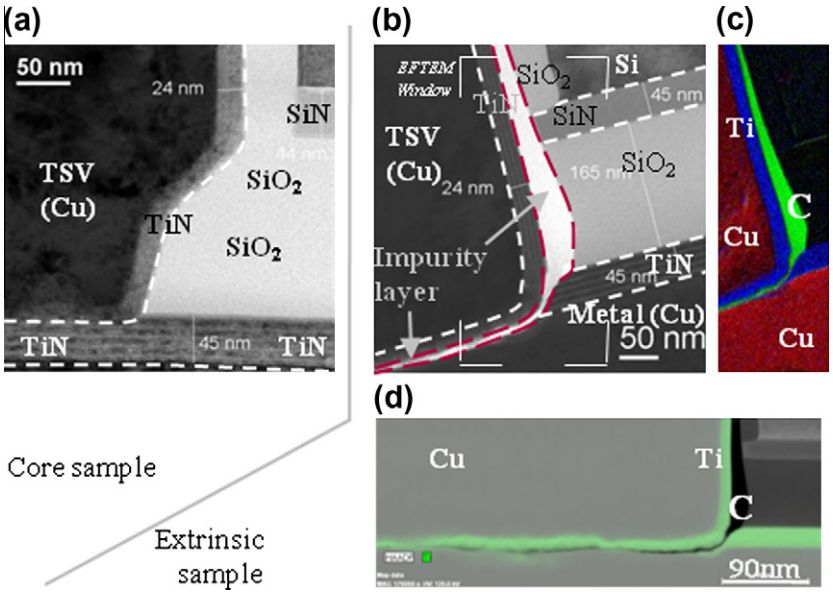

Fig. 4. Analyses of TSV bottom interface for core and extrinsic samples of a 2.3 μm TSV [10]: (a) TEM of a 2.3 μm core sample without impurity; (b) TEM of a 2.3 μm extrinsic sample with the impurity layer under the TiN; (c) EFTEM reveals the chemical presence of carbon in the impurity and (d) STEM of (b).

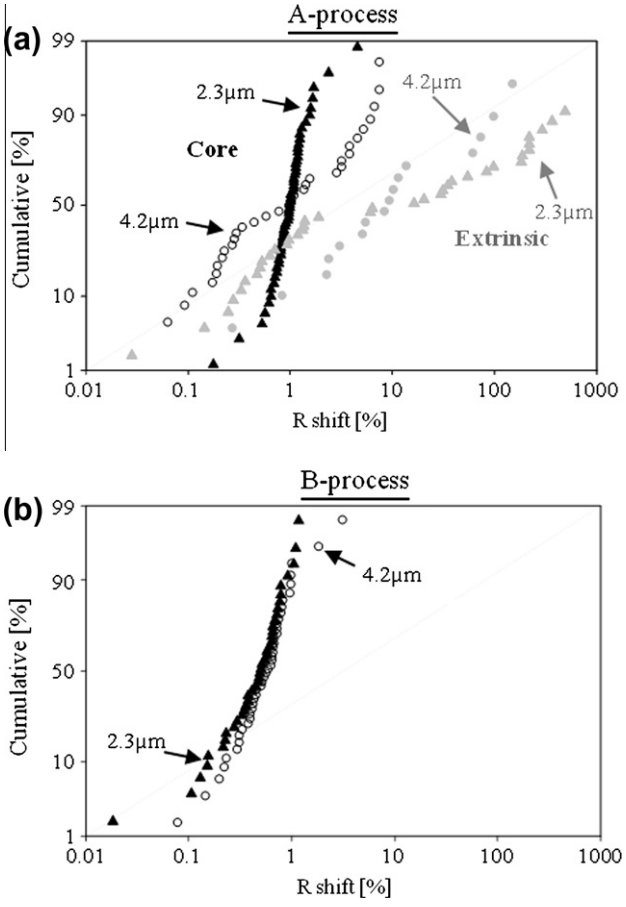

Fig. 5. Relative resistance change lognormal-plots after TC test: (a) A – process samples of 2.3 μm and 4.2 μm diameter TSV, for core and extrinsic populations and (b) B – process samples of 2.3 μm and 4.2 μm diameter TSV.

the zone are driven by the electron flow, as explained by [28]. The shape of the void showed in Fig. 8 indicates that the vacancy diffusion path is the Cu/SiN capping layer interface, which is known to be the weakest interface due to its high diffusion rate [29,30].

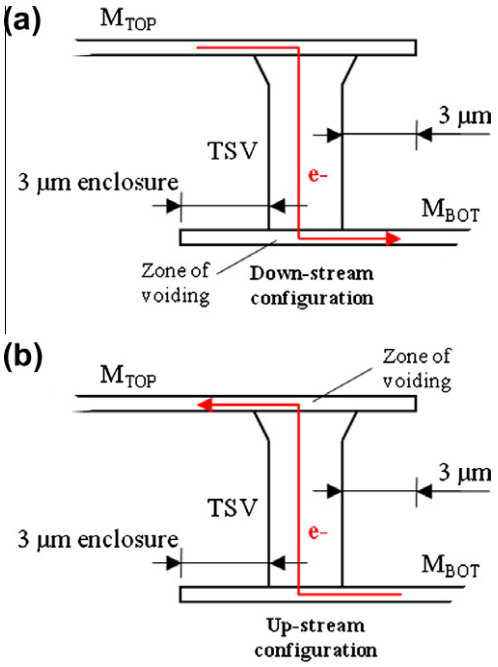

Fig. 6. Schematic of: (a) down-stream and (b) up-stream configurations for electromigration tests.

Table 1
Electromigration stress conditions.

Line process	Stress conditions		
Thin [0.25 μm] Down-stream	258 mA 300 °C	15 mA 300 °C	25 mA 270 °C
Thin [0.25 μm] Up-stream	25 mA 300 °C	15 mA 300 °C	25 mA 270 °C
Thick [3.0 μm] Down-stream	60 mA 300 °C	180 mA 300 °C	180 mA 270 °C
Thick [3.0 μm] Up-stream	60 mA 300 °C	*Not tested*	*Not tested*

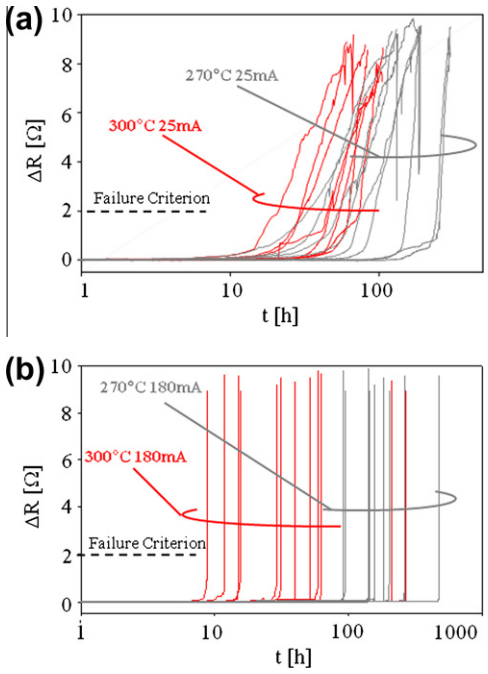

Fig. 7. Resistance traces for down-stream configuration of: (a) thin and (b) thick metal processes.

Failure analyses of thin process samples stopped during resistance increase reveal that the resistance increase occurs when the void becomes larger than the TSV conductive section, forcing the electrons to flow through the high resistive TiN barrier (Fig. 9a–d). Since the void spans over the whole line thickness, it is expectable that an increase of the metal level thickness should enhance EM performance.

Thick metal processed samples have also a void growth right above/under the TSV as for thin metal process (Fig. 9e–h). However the site of voiding is no more at the SiN interface, but at the metal line/TiN interface. We assume that the Cu/SiN capping interface is too distant from the divergence site of Cu atoms migration which is the TiN barrier at the transition between TSV and metal levels. Consequently, the critical depletion volume of Cu to open the conductive section under/above TSV does not span over the whole line thickness. Thus, a very thick line does not ensure an increase of depletion capability before failing because failure can be due to a slit void (Fig. 9 e–g), similar to ones also found in usual CMOS interconnects [31]. Moreover, concerning up-stream configuration, voiding are also observed at the opposite Cu/SiN interface (Fig. 9e and f). In addition, on down-stream configuration, analysis of a non-failed sample reveals that voiding can leave Cu under the TSV (Fig. 9h). EM voiding mechanism is thus more dispersed for thick metal level process than for thin metal level process.

2.3.3. Simulations of current density distribution

3D finite element simulations using COMSOL software are performed to compute the current density distribution on a down-stream structure, made of a TSV and an adjacent metal level. Cross section views in Fig. 10 reveal that thick metal line undergoes current crowding, leading to a more significant gradient in current density distribution along the vertical axis than for thin line. This gradient is assumed to drive the void nucleation at TiN interface under TSV.

Note that due to the difference of conductive section, maximal current density is located in the metal line for thin metal process, whereas it is in the TSV for thick metal process. However, no failure is found to be due to voiding located in the TSV, since similarly to the Blech effect, a strong back-flow is expected to avoid any significant Cu matter migration in the TSV [32].

2.3.4. Statistical approach

Time To Failure (TTF) are computed based on a failure criterion of $\Delta R = 2\ \Omega$ resistance increase. Both up- and down-stream configurations of thin metal processes have mono-modal TTF distributions and similar standard deviation confirming that failure is due to the same void mechanism. Up-stream configuration has

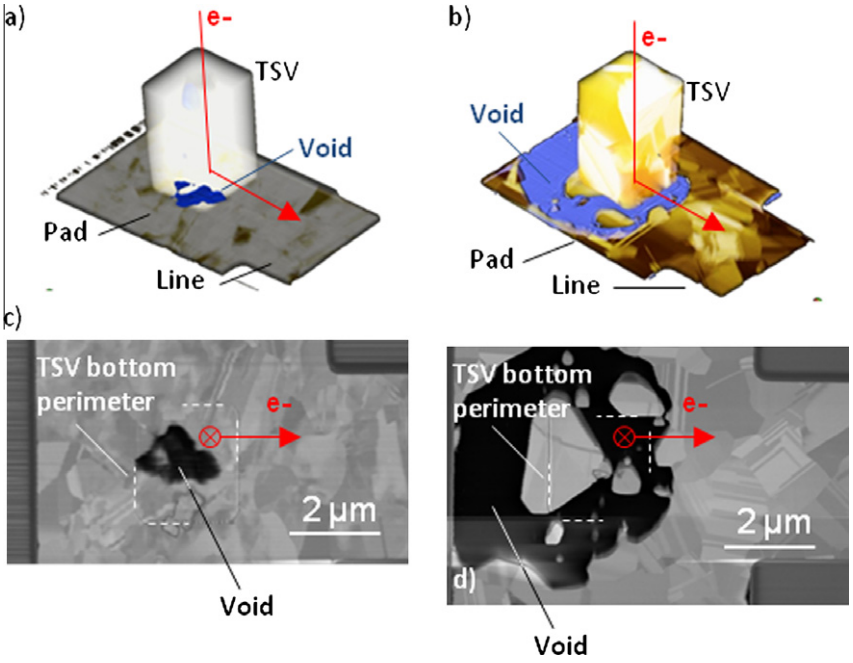

Fig. 8. 3D FIB-SEM reconstructed views: (a and c) sample stressed, but not until failure, and having no resistance increase: void nucleates and grows in metal level, right under TSV and (b and d) sample stressed until failure, and having resistance increase: void is now larger than TSV conductive section [17].

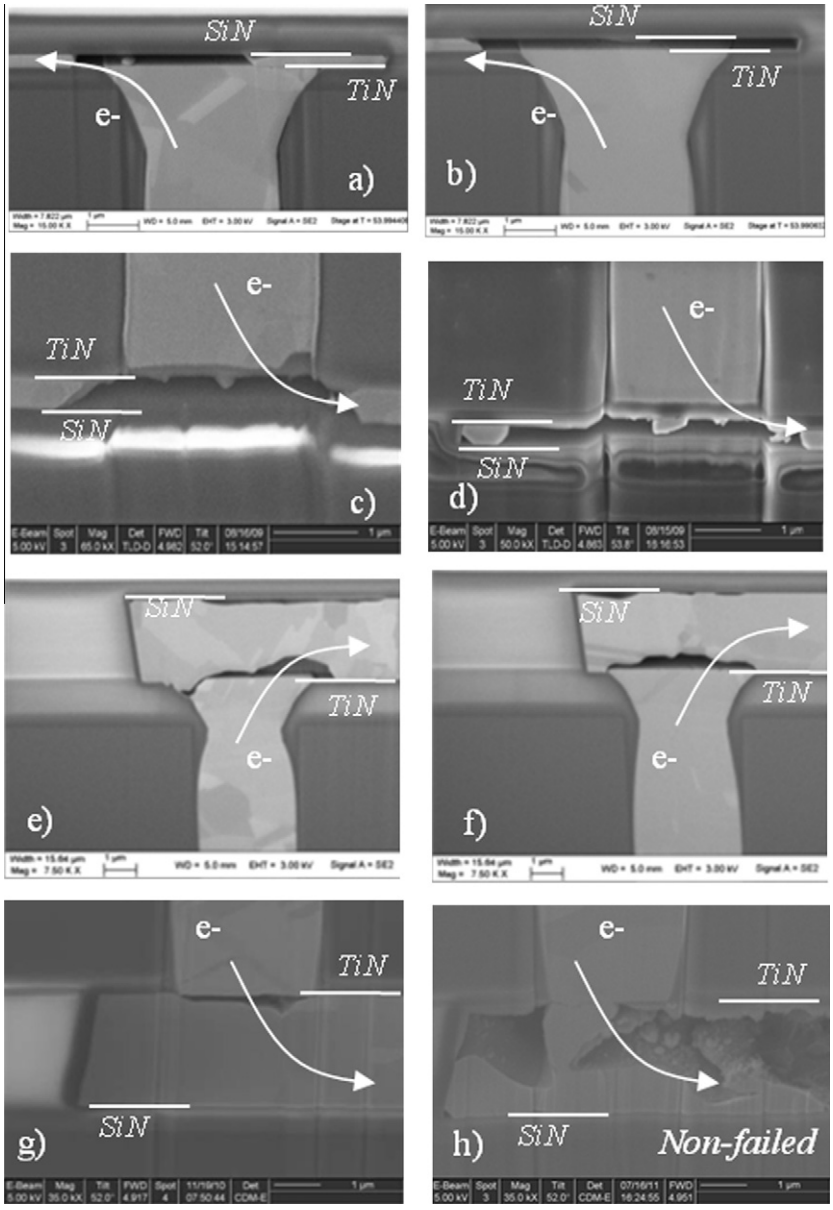

Fig. 9. Failure analyses of 2 samples for: (a and b) thin process up-stream; (c and d) thin process down-stream; (e and f) thick process up-stream and (g and h) thick process downstream.

about two times higher Mean Time to Failure (MTF) (Fig. 11). Following previously detailed failure analyses, the critical volume of depletion at which the resistance starts to increase is a cylinder having a diameter equal to the TSV diagonal and the thickness of the line one. The critical volume ratio of up-stream to down-stream is about 2 which is the computed MTF ratio of up- to down-stream.

For thick metal process, TTF distributions of both configurations are significantly more dispersed (Fig. 12). Actually, the void size at failure ranges from thin slit voids right at TSV interfaces, as in Fig. 9e, to very large volumes as in Fig. 9h, where even electrical open was not reached. Hence the dispersion on TTF distribution is strongly related to the void volume dispersion at failure.

2.3.5. Black's parameters estimation

Black's law, an empirical relationship, is used to link time to failure by electromigration, and the stress conditions of current density and temperature [33]:

$$MTF = Aj^{-n} \exp\left(\frac{E_A}{k_B T}\right) \quad (1)$$

where *MTF* is the median time-to-failure (time at which 50% of a tested samples have failed), *A* is a constant, *n* is the current density exponent, E_A is the activation energy, k_B is the Boltzmann constant, and *T* the stress temperature.

For thin metal process, current density exponent n and activation energy E_A of Black's equation are extracted through Time To Failure (TTF) data (Fig. 13). Very close values are obtained for both configurations. $E_A = 0.9 \pm 0.1$ eV is the expected activation energy for Cu damascene, ensuring that for both streams SiN capping is the major diffusion path. $n = 2 \pm 0.2$ is rather high regarding the theoretical value of 1 expected for Cu and might be the affected by local Joule heating in the TiN barrier as void becomes larger than the TSV section. As failure is revealed to be driven by void growth, any ageing extrapolations should be made with a consistent but conservative $n = 1$ [34].

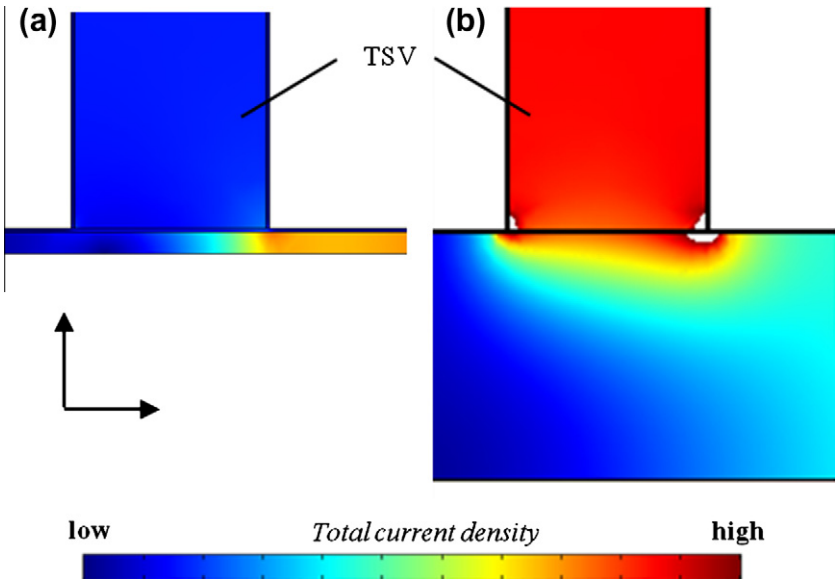

Fig. 10. Current density distributions concerning the down-stream structure: (a) thin metal process and (b) thick metal process.

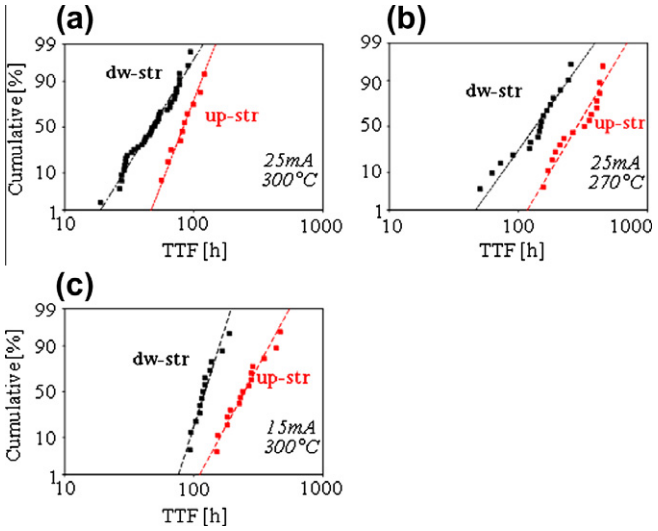

Fig. 11. Lognormal plots of TTF for thin metal level process for up- and down-stream structures at test conditions: (a) 25 mA–300 °C; (b) 25 mA–270 °C and (c) 15 mA–300 °C.

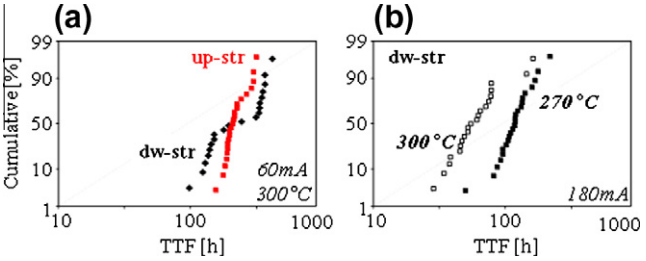

Fig. 12. Lognormal plots of TTF for thick metal level process: (a) up- and down-stream structures at 60 mA–300 °C; (b) down-stream structure at 180 mA–270 °C and 180 mA–300 °C.

For thick metal process, activation energy and current exponent for down-stream configuration are respectively of 0.8 ± 0.2 eV and 2.4 ± 0.3, which are close to values of the thin metal level process,

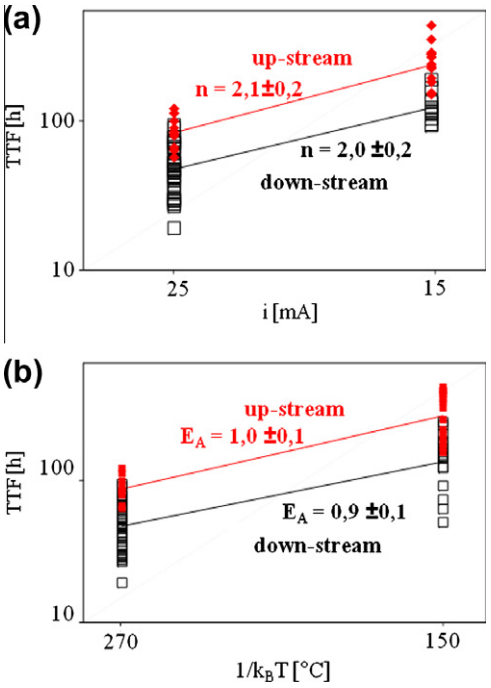

Fig. 13. Black's parameter extracted for up- and down-stream configurations of thin metal process: (a) current exponent n and (b) activation energy E_A.

but less accurate due to differences in lognormal standard deviation between TTF distributions.

With the same E_A = 0.9 eV, and a conservative n = 1, the TTF distributions of both thin and thick metallization processes are extrapolated at same operation conditions of current and temperature. At 50% cumulative failure, the benefit of thick metallization process is about 6 times higher than thin metallization process (Fig. 14). However, since lifetime is always extrapolated at 0.1% cumulative failure, thicker process has at this cumulative failure no significant benefit (only 1.1 times thin process).

Based only on current density considerations, thick metal process would have been expected to increase EM robustness. However, due to the void nucleation located right at TiN interface of

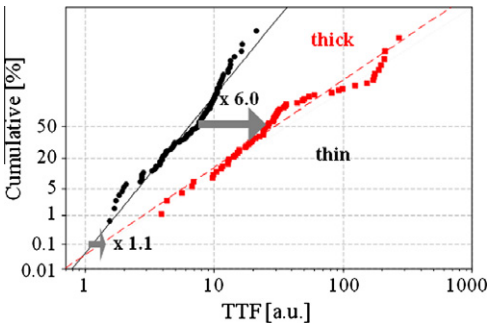

Fig. 14. TTF distributions of down-stream configuration, for both thin and thick metallization processes, extrapolated at operation conditions. At 0.1% cumulative failure, where lifetime is computed, thick line benefit is not significant.

TSV instead of opposite SiN capping layer, thick metal process fails mostly due to slit voids, without taking the benefit of a higher matter depletion capability. Moreover, since the void mechanism is dispersed – combining slit-voids and voids leaving Cu under the TSV – any lifetime extrapolation at low percentile is expected to be impacted by the worse dispersion. We expect thus that an increase of the line thickness enhances the EM performance only as long as the void spans over the line thickness before opening the conductive section of the TSV. Hence, there should be an optimal line thickness for which the maximum volume of Cu depletion is used before failure.

2.4. Combining TCT–EM and TS–EM

Since CTE mismatch between Cu and Si is suspected to induce stress at TSV interfaces, EM tests combined with Thermal Cycling (TC) ones (500 cycles of −65/+125 °C), or Thermal Storage (TS) of 250 h at 175 °C, are performed in order to ensure that EM voiding occurring at TSV interface is not enhanced by previous thermo-mechanical stresses. Tests are done on down-stream configuration of thin metal process. TSV process includes the enhanced pre-cleaning step. TTF distributions, of samples failed due to purely EM and samples failed due to EM but with TC as a pre-stress, reveal to be merged (Fig. 15). Same observation is made for samples having a TS stress previously to EM. Both results underline that preliminary TC or TS do not buildup any stress at TSV interfaces that significantly emphasize EM failure rate.

2.5. High density TSV-last conclusion

Reliability concerns of TC and EM on high density Cu TSV-last interconnects have been addressed in this first part. TC is a critical concern for only samples presenting initially imperfect interfaces. An optimized TSV process, enabling initial extrinsic-free resistance value distributions, ensures to pass TC assessment. TC is therefore expected to be not a critical concern for mature high density TSV-last process.

Electromigration tests performed on same TSV technology reveal that the site of void nucleation and growth is for up- and down-stream configurations respectively under and above the TSV in the corresponding metal level. The TSV section size at metal level interface is revealed to be critical for high electromigration performance. For thin metal level process, void at failure spans over the whole line thickness and the TSV section. Thick line process has a more dispersed voiding mechanism combining slit-voids and voids leaving Cu under the TSV. Therefore any thickness increase of metal level in order to increase directly the electromigration robustness should be considered carefully, since void nucleation interface and void growth can shift and strongly impact

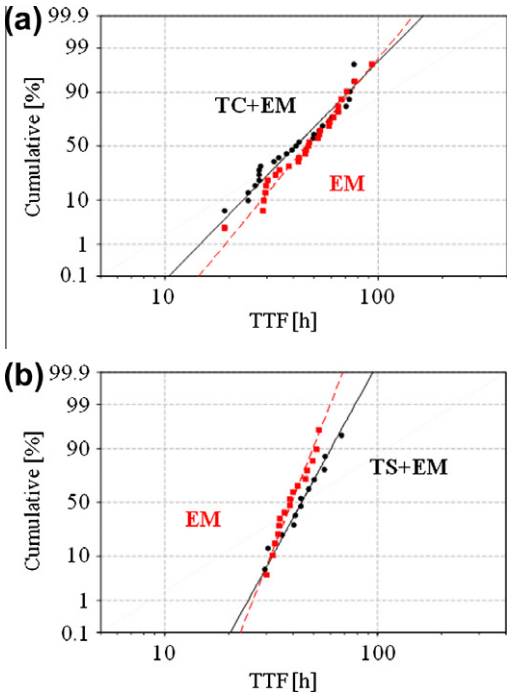

Fig. 15. TTF distributions of: (a) purely EM vs. EM + TC and (b) purely EM vs. EM + TS.

lifetime performances. Moreover, electromigration degradation is shown to be not accelerated by previous thermal cycling or thermal storage stresses.

3. Reliability of TSV middle

3.1. Process description

Similarly to above TSV-last test vehicles, a test vehicle based on TSV-middle approach has been designed and fabricated in a 65 nm CMOS node with six metal layers of BEoL. Cu TSV has a diameter of 10 μm and depth of 80 μm.

The main steps of the Cu TSV middle process are (Fig. 16): (1) TSV etching achieved with a Bosch Deep Reactive Ion Etching (DRIE); (2) deposition of a SiO_2 isolation layer, a Ta barrier deposition, Cu seed and electrolytic filling; (3) usual Cu damascene 65 nm node metal layers are finally processed and (4) after bonding, thinning, and flipping wafer, Redistribution Level (RDL) is processed for backside routing from the TSV. Cross-section of TSV with RDL at top is shown in Fig. 16. First process and electrical performances have been addressed in previous papers [27,35]. Concerning reliability, the test vehicle contains structures dedicated to address thermal cycling, electromigration, and BEoL dielectric breakdown stresses.

3.2. Thermal Cycling

Thermal Cycling (TC) assessments are performed on Kelvin TSVs, designed in two configurations: isolated TSV, and TSV surrounded by a dense patterning of dummy TSVs at minimum pitch (Fig. 17). Isolated and dense Kelvin TSVs are connected through 4-point measurement on RDL and first metal level (M1). Both configurations have two samples on each die. Initial resistance values (Fig. 18) reveal uni-modal distributions, without extrinsic samples, ensuring a mature TSV process. Both configurations have similar

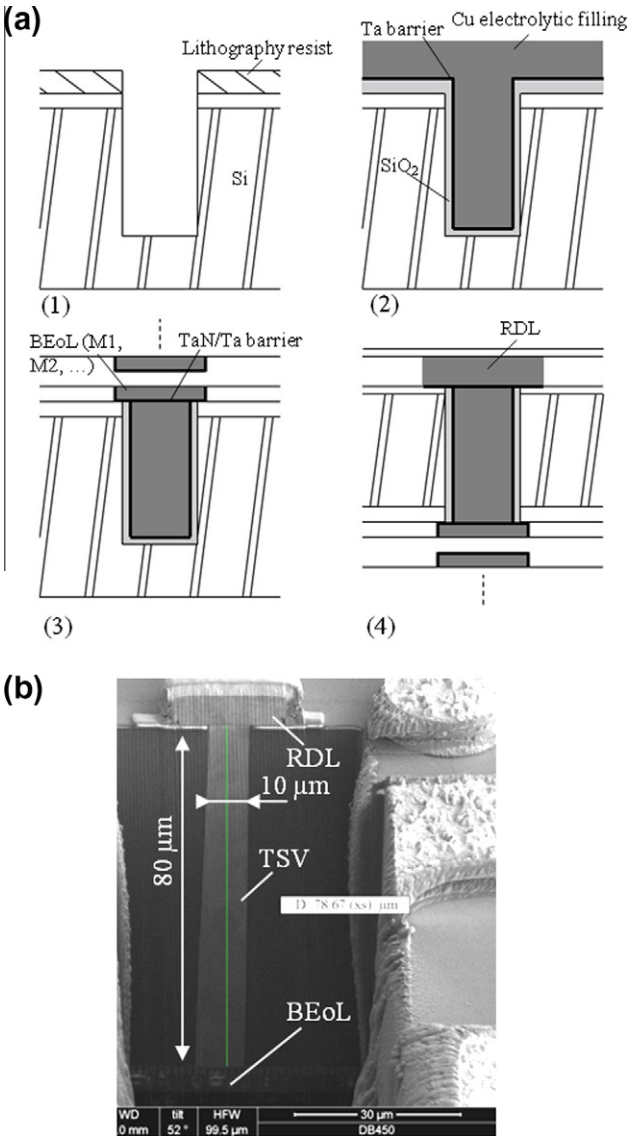

Fig. 16. (a) Schematic of TSV middle process steps and (b) SEM cross section picture of TSV.

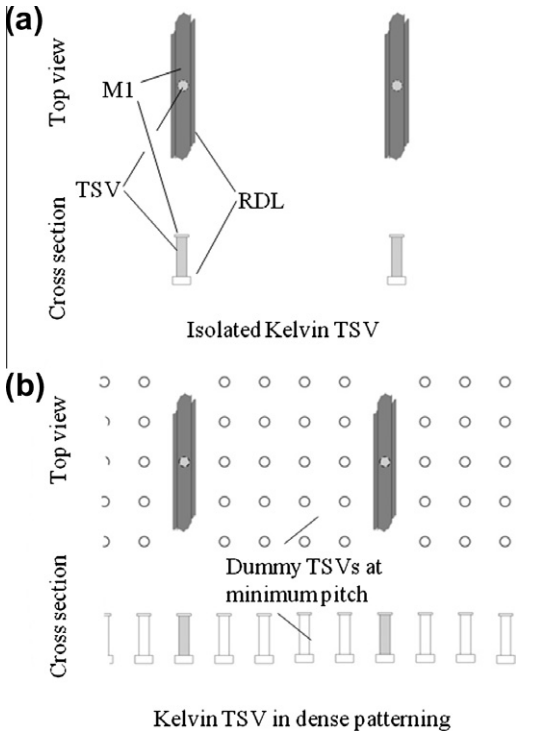

Fig. 17. Schematic of (a) isolated Kelvin TSV and (b) Kelvin TSV in a dense pattern.

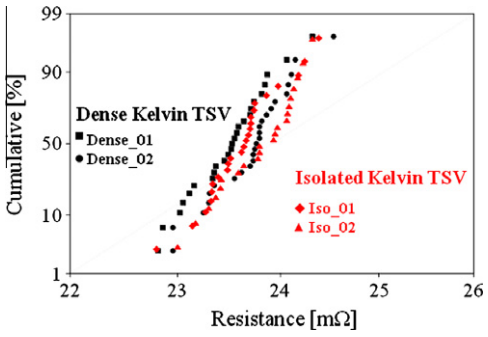

Fig. 18. Normal plots of initial TSV-middle electrical resistance, for both isolated and dense configurations. Both configurations have two devices on same die.

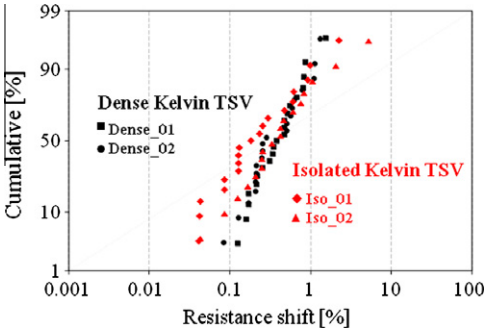

Fig. 19. Resistance shift plot after TC for both isolated and dense Kelvin TSV configurations.

dispersions. Isolated TSV have slightly higher resistance values, of about +0.1 mΩ (~0.5% relative shift) vs. dense TSV.

However, this very small difference is statistically not significant regarding distribution slope. Both configurations, subjected to 500 cycles of −65/+125 °C [25], have no significant shift, as plotted in Fig. 19.

3.3. Impact of TSV on BEoL dielectrics

Low-*k* dielectrics introduction in copper interconnects is a key point for the BEoL reliability [36–38], since wear-out due to dielectric breakdown becomes a main concern. Although 65 nm node technologies are today mature, and in high volume production, the eventual impact TSVs on adjacent low-*k* inter metallic dielectric has to be assessed through Time Dependent Dielectric Breakdown (TDDB) analysis.

In this study, copper dual damascene structures were fabricated in 65 nm technology node process with a SiOCH low-*k* dielectric (dielectric constant of $\varepsilon_r = 2.9$). Chemical Mechanical Polishing (CMP) stops on a Tetra-Ethyl-Ortho-Silicate (TEOS) layer.

The test structures are interdigited combs at metal 2 (M2) and metal 3 (M3) levels with a space of 100 nm, a width of 100 nm and a structure length of 8000 µm. Combs having three TSVs right below, as depicted in Fig. 20, are compared to references combs. All

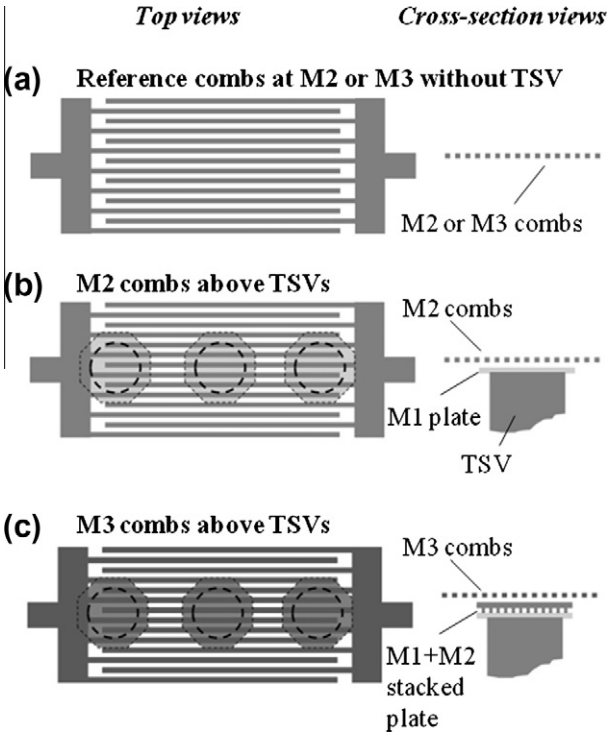

Fig. 20. Schematic of tests structures to study the impact of TSV on TDDB of above BEoL levels: (a) M2_ref, and M3_ref; (b) M2_TSV; (c) M3_TSV.

four structures (M2_ref, M2_TSV, M3_ref, M3_TSV) are designed and tested within the same die-field. TSV pad consists of a 12 µm large M1 plate for M2_TSV and a stack of 12 µm large M1 and M2 plates connected by vias for M3_TSV structure.

Constant Voltage Stress (CVS) stresses are performed at 25 °C at two voltages of 55 and 60 V. Failure criterion is the abrupt jump of the monitored leakage current. Weibull distributions of TTF are plotted in Fig. 21 and reveal that for both 55 and 60 V stresses, M2 configuration has about 30% lower MTF with TSV than without TSV. Concerning M3 level, TTF distributions of both configurations of with- and without-TSVs, are merged.

The difference in TTF between the M2_ref and the M2_TSV structures is either related to the presence of the TSV, or the pad consisting of a 12 µm diameter M1 plate. Since M3_ref and M3_TSV have merged TTF distributions, it is expected that a 12 µm plate at n level do not impact the TDDB of n + 1 level. Therefore, only the presence of the TSV explains the differences between M2_ref and M2_TSV.

The robustness of low-k dielectric is generally assumed to be impacted by four items, related to topology of lines, and depicted in Fig. 22: (1) intrinsic performances of the SiOCH/TEOS interface, since trapezoidal shape of lines, due to the SiOCH etching, leads applied electrical field and resulting current leakage to be higher at this interface [37]; (2) the characteristic and thickness of TEOS, impacted by CMP polishing [36]; (3) intrafield line to line spacing dispersion, related to photolithography fluctuations [37]; (4) line edge roughness (LER), already reported as first-order reliability detractor for TDDB of low-k dielectrics [37–39].

Regarding the design of test structures, the four devices are within the same die-field, and any photolithography or LER fluctuations between M2_ref and M2_TSV should be also significant between M3_ref and M3_TSV. We exclude therefore points (3) and (4), and expect that the difference of TDDB performance between M2_ref and M2_TSV is related to the impact of TSV on points (1) and (2). Since TSV is in a tensile stress state at 25 °C [40], which

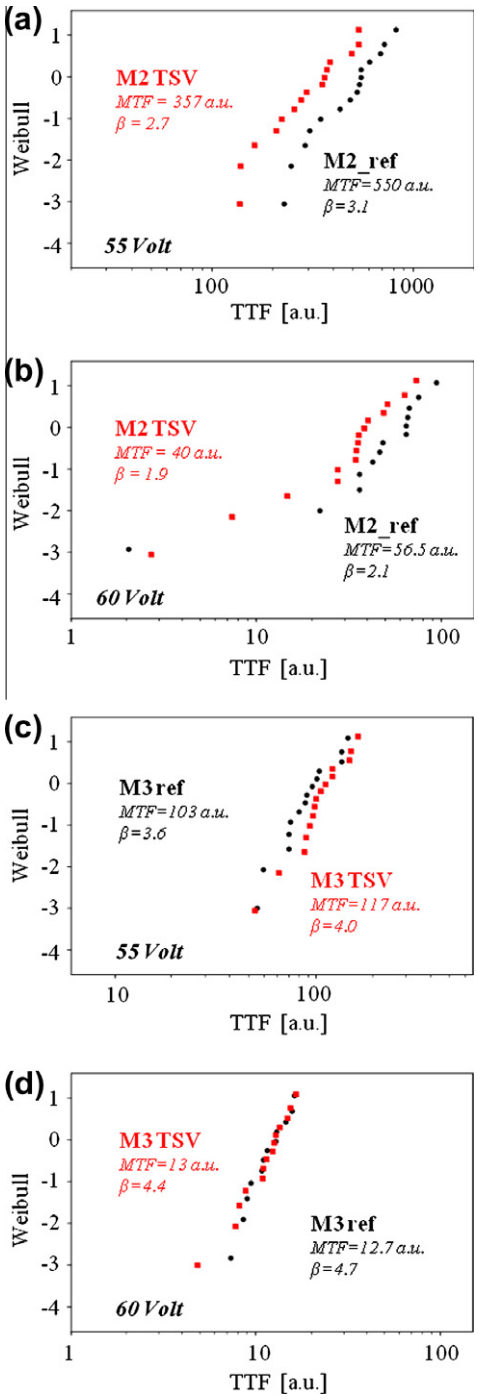

Fig. 21. TTF distributions of CVS stresses: (a) Metal-2 reference combs (M2_ref) vs. Metal-2 combs above TSVs (M2_TSV) at 55 Volt; (b) Metal-3 reference combs (M3_ref) vs. Metal-3 combs above TSVs (M3_TSV) at 60 Volt.

is the temperature of M2 CMP step, it is expected that the TEOS thickness may shift in an environment where TSVs are below. Moreover, tensile stress of TSVs, may create also more initial defects at SiOCH/TEOS interface of M2 level, accelerating the dielectric breakdown.

The merged distributions of M3_ref and M3_TSV underline that any tensile stress due to TSV has no effect at this metal level. Routing wires above TSV can therefore be considered as safe for M3 or upper metal levels.

To conclude, the TSV presence is revealed to be significant for TDDB of M2 dielectrics. However, regarding the intrinsic perfor-

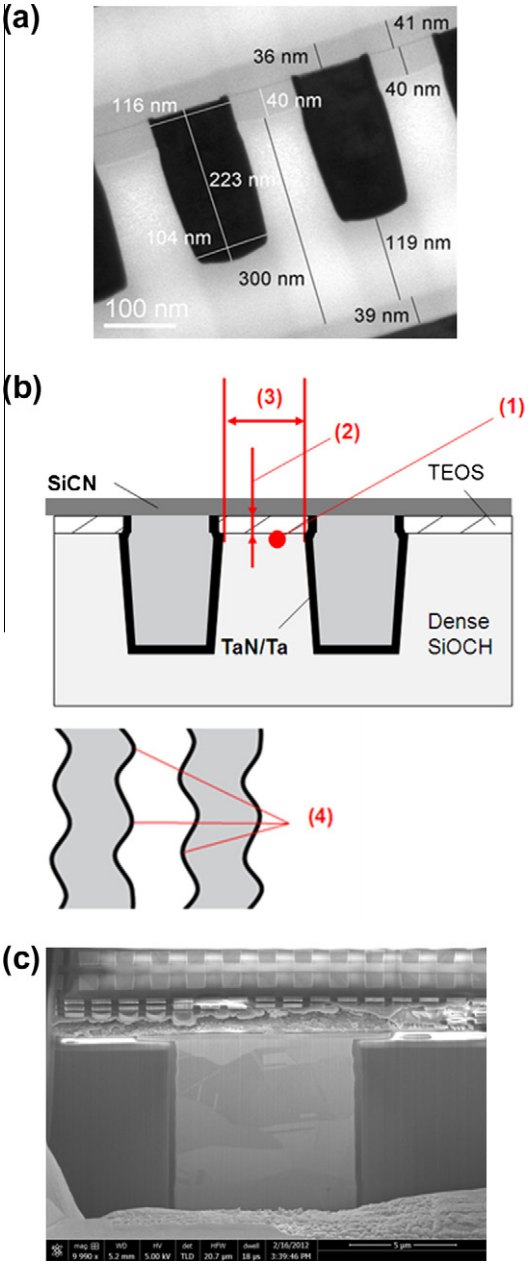

Fig. 22. (a) TEM cross section of Cu dual damascene metal levels for the 65 nm node. (b) Schematic cross section and top view of line to line, with numbers pointing on items impacting TDDB. (c) SEM cross section of M2_TSV structure after dielectric breakdown due to 60 Volt CVS.

mances of the mature 65 nm node, a lifetime reduction of even 30% induces no critical reliability issue. Nevertheless, the introduction of porous low-*k* in more advanced nodes, i.e. below 45 nm node, associated with the reduction of the line to line spacing, is assumed to be more sensitive to any impact of TSV on TDDB performances.

3.4. Electromigration

Electromigration stress at TSV/M1 interface is performed at package level. TSV has a 10 µm diameter and M1 is 12 µm wide and 180 nm thick. Structure is schematically depicted in Fig. 23. At M1 level, TSV has a 1 µm large enclosure.

Electrical resistance traces are similar to ones monitored for high density Cu TSV-last: first latency period followed by an

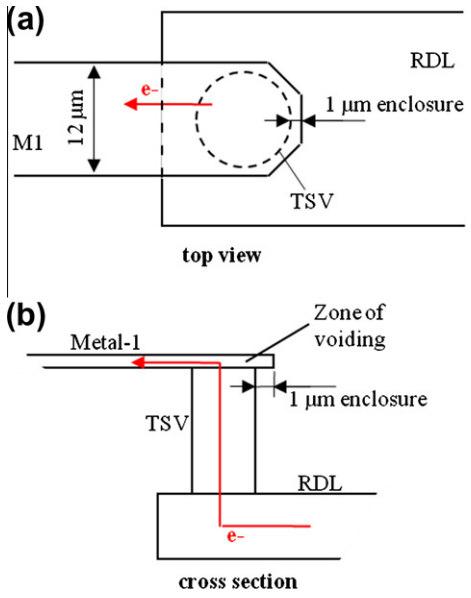

Fig. 23. Schematic of electromigration structure at TSV/M1 interface: (a) top view and (b) cross section view.

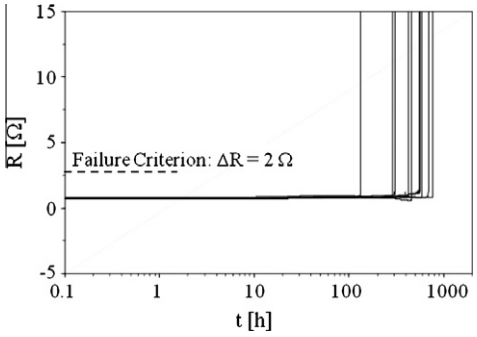

Fig. 24. Resistance trace monitored under 300 mA–300 °C stress.

increase (Fig. 24). Failure analyses made on two samples before resistance increases reveals a void in M1, right under TSV, close to its perimeter. From cross section views of void shape, the nucleation and Cu diffusion appears to be located at the Cu/SiCN capping interface of M1 (Fig. 25). This nucleation interface is expected to be best case to maximize performance, since the consequent volume at failure will have whole M1 thickness. No slit-void behavior is expected to occur at TSV/M1 interface.

Regarding a statistical approach, the TTF distribution of 10 samples stressed until electrical open, has a uni-modal slope, underlining a single mode failure (Fig. 26). Based on activation energy of $E_A = 0.9$ eV, representative for Cu diffusion at Cu/SiCN, and a conservative current density exponent of $n = 1$, the extrapolated lifetime at 125 °C for 0.1% cumulative failure exceeds the 10 year target at operation current condition.

3.5. TSV-middle conclusion

Reliability concerns of TC, TDDB of adjacent BEoL, and EM have been addressed in this second part for a Cu TSV middle technology. The mature TSV process enables to pass TC assessments. TSV is revealed to have an impact on M2 TDDB of low-k dielectrics. However, no impact is measured for higher metal levels, i.e. M3. Analysis of electromigration at TSV/M1 points out that the site of

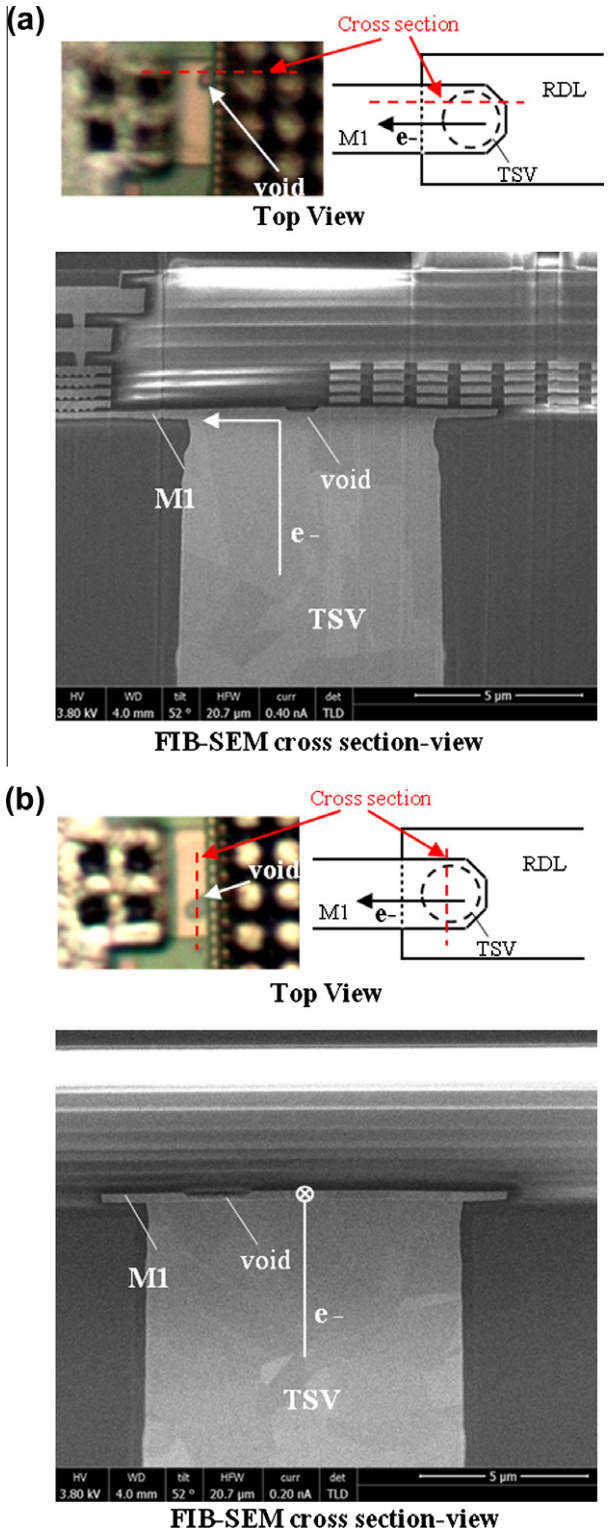

Fig. 25. SEM cross section views of two samples, at TSV/Metal-1 interface. EM stress stopped before resistance starts to increase: (a) SEM cross section aligned with M1 line and (b) SEM cross section vertical to M1 line.

void nucleation and growth is located in M1, right under the TSV, with a diffusion and nucleation interface at the capping layer. Regarding previous study on high density Cu TSV-last, the void nucleation and growth behavior ensures to benefit from whole M1 thickness before opening the conductive section.

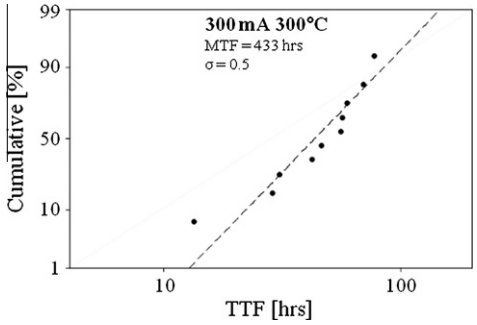

Fig. 26. TTF distribution at 300 mA and 300 °C. Failure criterion is set to $\Delta R = 2\ \Omega$.

4. Conclusion

In this paper, reliability of Through Silicon via (TSV) interconnects is analyzed for two technologies: high density Cu TSV-last and Cu TSV-middle. For both technologies, mature processes ensure to pass Thermal Cycling assessments for Kelvin TSV devices. Studies of electromigration behavior reveal that for both technologies, voiding is located above the TSV, in the adjacent metal level. In case of usual thin metallization level, void nucleation and Cu diffusion under electromigration occur at the capping layer, leading to expect comfortable lifetime at operation conditions. Time Dependent Dielectric Breakdown analyses of first BEoL metal levels point out that below TSV may impact second metal level dielectric performance. However, higher metal level dielectrics are shown to be not impacted by the presence of TSV.

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