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Thermal expansion behavior of through-silicon-via structures in three-dimensional microelectronic packaging

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ABSTRACT

Thermo-mechanical reliability is an important issue for the development and deployment of the through-silicon-via (TSV) technology in three-dimensional (3D) microelectronic packaging. The mismatch in coefficient of thermal expansion (CTE) between the array of copper (Cu) lines and the surrounding silicon (Si), upon temperature variation, affects the overall thermal expansion behavior of the whole TSV structure itself and generates an internal stress state. In this work we use the finite element method to numerically study the effective in-plane CTE of the Si/Cu composite structure. A 3D unit-cell approach is undertaken, which takes into account uniformly distributed TSVs in the Si chip. Results of the temperature-dependent effective CTE can be used as model input for simulating larger-scale 3D packages where the Si/Cu TSV structure is treated as a homogeneous material. We also examine the evolution of stress and deformation fields, and identify potential reliability concerns associated with the thermal loading.

1. Introduction

Three-dimensional (3D) integration has emerged to be the enabling technology to further the advancement of microelectronics. The enhancement of device density/capacity per volume, utilization of short vertical interconnection for improved electrical performance, and capability of integrating heterogeneous functions in a single package characterize some of its unique advantages [1–3]. At the heart of 3D integration is the through-silicon via (TSV) technology. TSVs are typically metal filled vertical line arrays in a thinned silicon (Si) chip, which provide the signal paths between the stacked chips. Fig. 1a shows a schematic of stacked Si chips with copper (Cu) TSVs. In between the chips the TSVs are connected through solder bumps. Larger solder bumps are used for joining the packaging substrate and the chip stack. Underfill material may be applied, and there are adjacent support and heat conducting structures (not depicted in the figure).

In many circumstances it is difficult to incorporate TSVs in an active chip, due to the very high density and complexity of device features [4]. Stresses in Si caused by the mismatch in coefficient of thermal expansion (CTE) between Cu and the surrounding Si may also have detrimental influences on the electronic performance [5]. The use of TSV structure as a passive interposer may be an effective remedy, as schematically shown in Fig. 1b. In this example the interposer anchors two active chips (may be of different functionalities) and directs the signals to the packaging substrate. There is also an added benefit of this arrangement: reducing the cracking propensity in the on-chip low-k dielectric material caused by thermal expansion mismatch between the Si chip and organic substrate. This is because the CTE mismatch between the Si chip and TSV interposer is much reduced [2]. Note, however, that thermal stresses are still generated between the interposer and packaging substrate. Solder joint failure is also of concern as in traditional packages.

Aside from the thermo-mechanical reliability issues, thermal management presents another critical challenge. The total power generation per unit surface area is much greater in the 3D structure, and it becomes more difficult to implement effective cooling mechanisms [4]. Comprehensive thermal and mechanical analyses are thus required, which calls for large computational finite element models with sophisticated structural features incorporated. For the types of TSV structure depicted in Fig. 1 (in active chips or as a passive interposer), it is apparent that treating the Si/Cu assembly as a composite material, rather than including all the Cu features along with the surrounding Si, is a practical approach, to avoid the prohibitively large number of degrees of freedom in an extremely finely meshed model. This involves obtaining the effective material property, such as CTE, for the TSV structure. Note that there is a large difference between the CTE of Si (about $3 \times 10^{-6}/°C$) and that of Cu (about $17 \times 10^{-6}/°C$). Indeed the effective CTE of TSV structure has become a matter of interest in recent studies. For instance, analytical formula pertaining to continuous fiber reinforced composites has been adopted as model input for the transverse (in-plane) effective CTE of Cu TSV-containing Si [6]. However, fiber composites are under the generalized plane strain condition because of their much greater dimension in the fiber length direction compared to the geometric features in the transverse direction. Therefore it is not representative of

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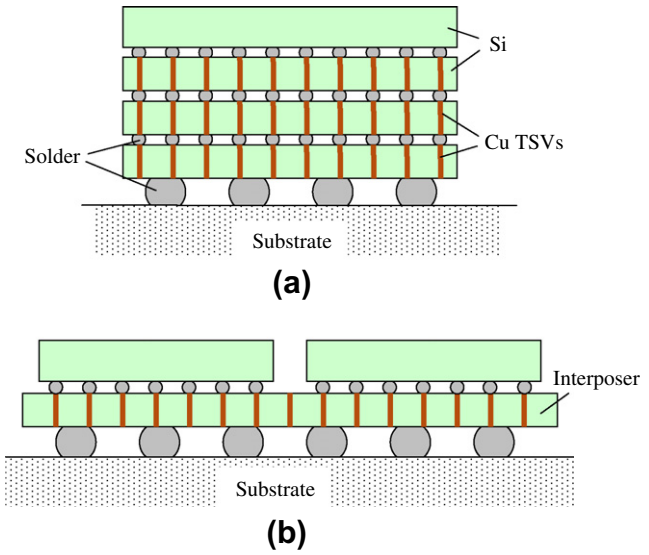

Fig. 1. Representative 3D integration schemes: (a) vertical stacking of Si chips containing Cu TSVs, and (b) an interposer used between two Si device chips and packaging substrate. The schematics are not to scale, and the possible underfill material and other peripheral structures are not included.

typical TSV structures. In the same study [6], using effective CTE as one of the design parameters to achieve optimal design was also proposed. Other authors have assigned a value of $10 \times 10^{-6}/°C$ (midway between Cu and Si) for the TSV-containing interposer in their finite element analysis [4]. Clearly there is a need to quantify the effective CTE for such purposes, especially with the lack of analytical models and experimental data for the TSV structure.

The present work is devoted to numerical characterization of effective CTE of the Si/Cu TSV structure. Owing to the component layout (Fig. 1) the in-plane CTE value is most relevant, and thus will be the focus here. The specific objectives include:

- To quantify the CTE as affected by TSV area fraction, TSV height (wafer thickness), and temperature, which can serve as reliable input information for modeling larger-scale 3D packages.
- To examine the stress and deformation fields in the Cu TSV and Si matrix induced by their thermal mismatch, and thus assess the mechanical integrity of the TSV structure itself.

It is noted that, in addition to the effective CTE, the overall elastic modulus is also needed when treating the Cu/Si composite structure as a homogeneous material in large-scale modeling. Nevertheless, the elastic modulus is not studied here because the moduli for Cu and Si are not very different and the effective value will thus be within a close range regardless of the TSV area fraction. The present work therefore only considers CTE as motivated by the issues raised in recent studies [4,6] described above.

2. Model description

The 3D unit-cell model is used to simulate the Cu TSV-containing Si chip, with deformation induced by prescribed temperature variation. Fig. 2a shows the in-plane periodic array of the Cu lines. The barrier layer between Cu and Si is ignored in the current baseline study, as its effect on the overall CTE will be negligibly small if the layer is sufficiently thin. Although in reality a 3D device may not have a true regular periodic array of Cu TSV lines with perfectly vertical side walls throughout, the present assumption serves the purpose of allowing the extraction of effective CTE values influenced by the overall TSV content and other associated geometric features. Without such an assumption it is also difficult to assess the local

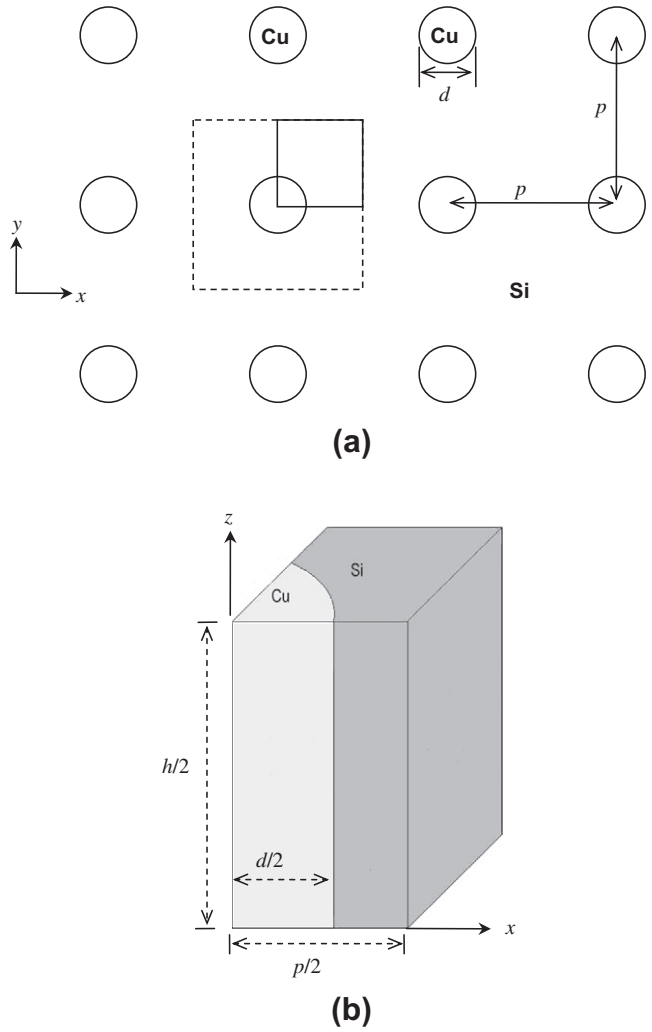

Fig. 2. (a) Top view of the periodic arrangement of Cu lines in Si matrix; the dashed square is a full unit cell, but only a quadrant is needed for the modeling, and (b) 3D computational domain used in the modeling. The parameters p, d and h represent the pitch, Cu diameter and TSV height, respectively.

stress and deformation fields in a systematic way. A square arrangement is assumed [5,7–9], with the line diameter and pitch being d and p, respectively. The dashed square in the figure shows a full unit cell, only a quadrant of which is used in the modeling with the appropriate boundary conditions applied. (It is noted that, with the symmetry condition only one eighth of the unit cell is actually needed. However, due to visual convenience for model setup and output analysis we chose to include a quadrant.) The actual computational domain, shown in Fig. 2b, includes only one half of the TSV height. Thus the three boundary planes, $x = 0$, $y = 0$ and $z = 0$, are symmetry planes with displacements in x, y and z, respectively, prohibited during deformation. Tangential movements of nodal points in these planes are allowed. The top surface, $z = \frac{h}{2}$, is unconstrained. The other two side-surfaces, $x = \frac{p}{2}$ and $y = \frac{p}{2}$, are allowed to move in a parallel manner, so that the x-direction movement of the plane $x = \frac{p}{2}$ and the y-direction movement of the plane $y = \frac{p}{2}$ are both uniform. These boundary conditions preserve the periodicity and symmetry of the entire structure, and allow for quantification of deformation caused by the thermal expansion mismatch between the regularly arrayed Cu TSVs and Si matrix. The in-plane CTE (along the xy-plane) of the composite, α_c, is then expressed as

$$\alpha_c = \frac{2u}{p \cdot \Delta T}, \tag{1}$$

Table 1
Material properties used in the finite element modeling (E: Young's modulus, ν: Poisson's ratio, α: coefficient of thermal expansion, σ_y: yield strength, H: plastic linear hardening slope). A linear variation of properties with temperature between the indicated temperatures is assumed.

	Cu	Si
E (GPa) at 20 °C	110	130
400 °C	103.1	130
ν at 20 °C	0.3	0.28
400 °C	0.3	0.28
α (10^{-6}/K) at 20 °C	17.0	3.1
400 °C	19.6	4.7
σ_y (MPa) at 20 °C	155	–
400 °C	99.3	–
H (GPa) at 20 °C	17.8	–
400 °C	2.6	–

where u is the displacement in x of the plane $x = \frac{p}{2}$ (or equivalently, displacement in y of the plane $y = \frac{p}{2}$), and ΔT is the temperature change.

The Si matrix in the model is assumed to be an isotropic linear elastic solid. The Cu line is taken to be isotropic elastic–plastic with linear strain hardening, with its plastic yielding following the von Mises criterion and incremental flow theory. The temperature-dependent material properties used in the modeling are listed in Table 1 [10]. The plastic yielding behavior of Cu is based on experimental measurement of a 1 μm-thick passivated Cu film [11]. Note that when conducting stress modeling involving metal in device structures, it is important to incorporate the plastic deformation feature in the model even if the metal is under physical confinement [12–14]. This is because that, with more realistic material properties incorporated, more accurate local stress distributions can be obtained, and the quantitative plastic strain information is a good indication of damage propensity. For instance, in regions where intensive plasticity is found, the concentration of crystal defects can be expected. Subsequent void nucleation may thus preferentially occur in those regions.

In the present model the Cu lines and Si are assumed to be perfectly bonded so the displacement field across the interface is continuous. Thermal loading is simulated by imposing a spatially uniform temperature excursion. Two ranges of temperature change are considered for the determination of composite CTEs: 20–50 °C and 20–320 °C. When analyzing the mismatch induced internal deformation fields, a cooling scenario from 320 to 20 °C is also considered. In all cases the stress-free state is assumed to exist at the initial temperature. Note that the stress-free temperature will affect the evolution of internal thermal stresses (as presented in Section 3.2). For CTE calculation, taking 20 °C as the stress-free state is a reasonable first choice because, from previous modeling analyses of metal-ceramic aggregates, incorporating a processing step and thus a different initial temperature will only affect the overall CTE slightly especially in cases where the ductile metal is surrounded by the elastic ceramic [15]. The finite element program Abaqus (Version 6.8, Dassault Systemes Simulia Corp., Providence, RI) is employed for the computation. A total of 28,860 eight-noded linear elements are included in the model, with a finer mesh size near the interface and free surface.

In general, the composite CTE will be affected by the dimensions and spatial distribution of the TSVs. For the unit-cell model used in the present study, the CTE values will be determined by the overall area fraction of the Cu TSVs under a fixed model height. In addition, there is no intrinsic length scale in the finite element analysis. Therefore, when presenting the results we will use two parameters to completely define the geometry: area fraction of Cu, $\frac{d^2\pi}{4p^2}$, and aspect ratio of the unit cell, $\frac{h}{p}$. For easy referencing with regard to the area fraction, we show in Fig. 3 direct correlation between the TSV area fraction and the actual values of TSV diameter d, for four representative values of the pitch p. For example, if the TSV diameter and pitch are 20 and 100 μm, respectively, the area fraction is then approximately 3%.

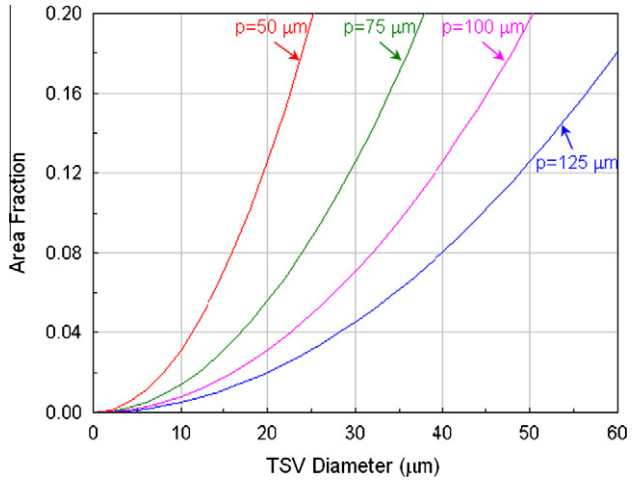

Fig. 3. Area fraction of TSV as a function of its diameter, for the square-arrayed TSVs with pitches 50, 75, 100 and 125 μm.

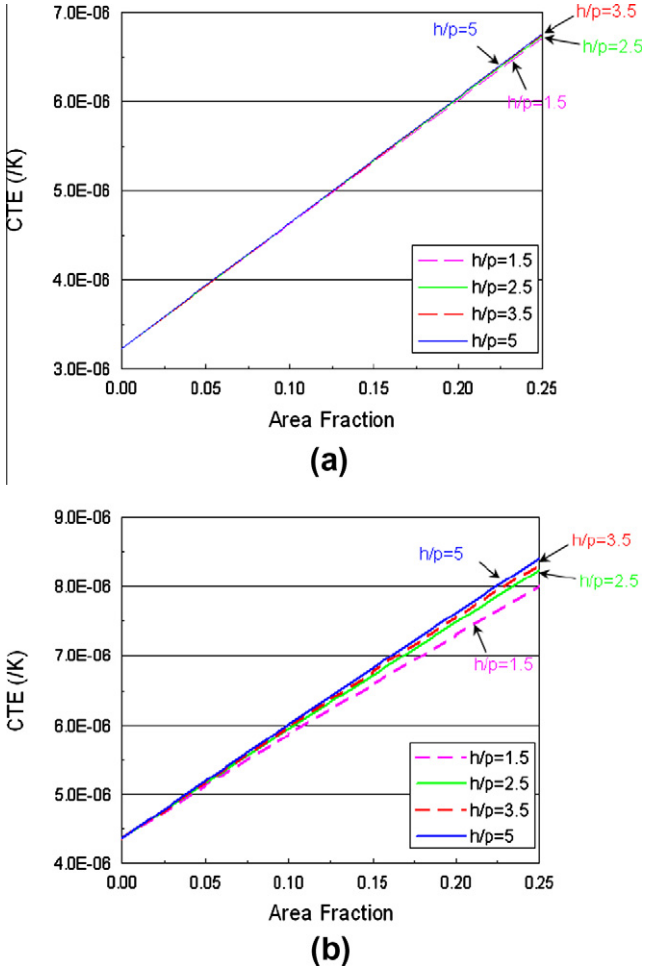

Fig. 4. Effective CTE as a function of TSV area fraction, when the temperature change is from 20 to (a) 50 °C and to (b) 320 °C. Four aspect ratios of the unit cell are considered: 1.5, 2.5, 3.5 and 5.

3. Results and discussion

3.1. Effective CTE

In this section the modeling result of effective CTE is presented. Fig. 4a shows the CTE as a function of TSV area fraction, for the case of heating to 50 °C. It can be seen that the CTE increases with Cu area fraction, because of the greater CTE of Cu compared to Si. The curves appear close to linear. The four aspect ratios of the unit cell considered, $\frac{h}{p} = 1.5, 2.5, 3.5$ and 5, result in very close values at any given area fraction (although numerically the effective CTE is higher for a higher $\frac{h}{p}$).

Depending on the temperature range of interest, the near room temperature analysis presented above may not be applicable. The result for a higher-temperature case, of heating to 320 °C, is shown in Fig. 4b. In the entire range of area fraction the CTE values are higher than those shown in Fig. 4a, due to the fact that the temperature-dependence of Cu and Si properties is incorporated in the model (specifically, the CTE of the constituents inherently increases with temperature). The difference observed between Fig. 4a and b ranges from about 1.2 to 1.7×10^{-6}/°C. In Fig. 4b the individual curves from the four aspect ratios are discernible, especially when the Cu area fraction is higher. At a greater aspect ratio, there is a larger fraction of Cu material away from the free surface or under higher interfacial constraint (and thus becoming more restricted in out-of-plane expansion), which results in somewhat greater lateral expansion and hence the higher in-plane effective CTE.

The results in Fig. 4 illustrated that, although the curves are not strictly straight lines, they can be approximated by a linear form with only minor influence from the ratio $\frac{h}{p}$. Thus for practical purposes the composite CTE, α_c, can be treated as following the rule of mixtures,

$$\alpha_c = f\alpha_{Cu} + (1-f)\alpha_{Si}, \tag{2}$$

where f is the area fraction of Cu and α_{Cu} and α_{Si} are the CTEs of Cu and Si, respectively. With the temperature-dependence included, α_{Cu} and α_{Si} are expressed as

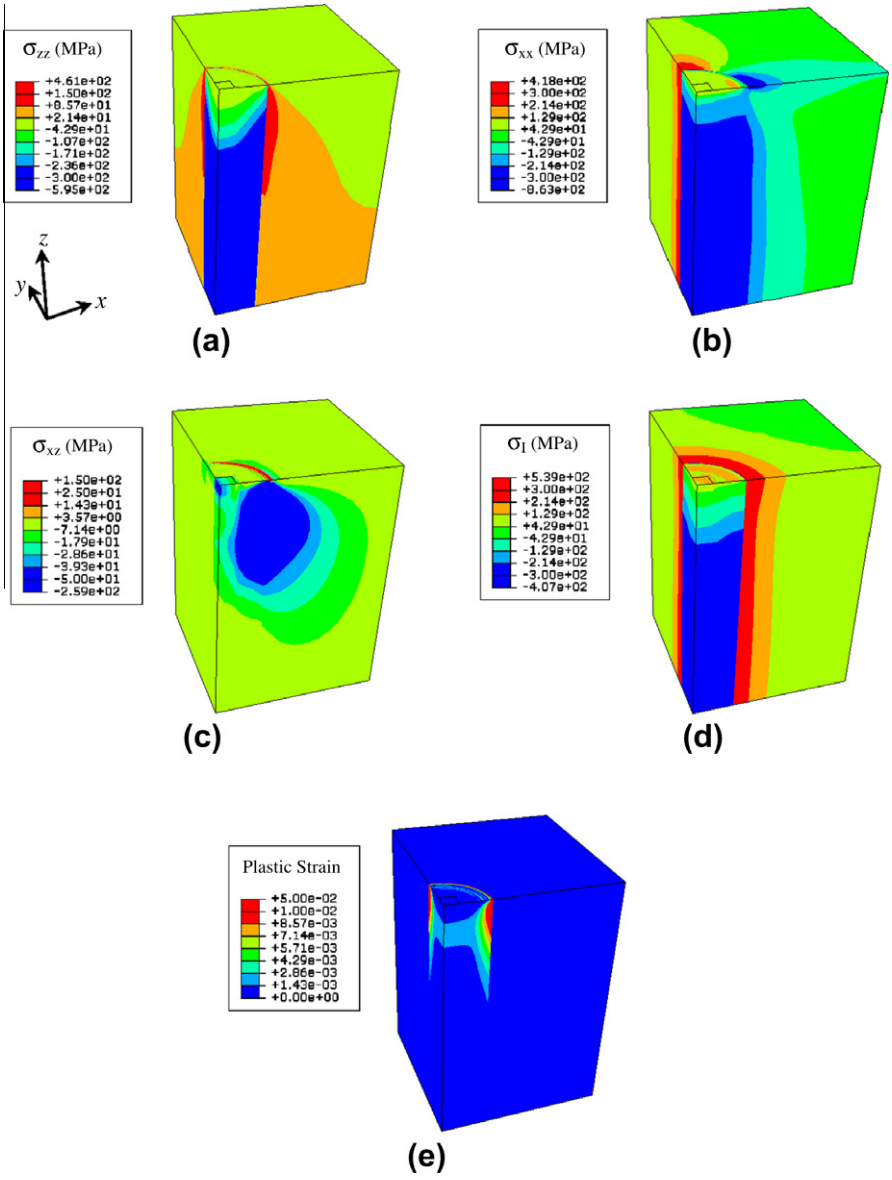

Fig. 5. Contour plots of (a) normal stress σ_{zz}, (b) normal stress σ_{xx}, (c) shear stress σ_{xz}, (d) maximum principal stress and (e) equivalent plastic strain, in the TSV structure with 0.05 area fraction of Cu and $h/p = 1.5$, after heating from 20 to 320 °C.

$$\alpha_{Cu} = [16.863 + 0.00684T] \times 10^{-6}, \quad (3)$$

$$\alpha_{Si} = [3.016 + 0.00421T] \times 10^{-6}, \quad (4)$$

where T is temperature in °C, and α_{Cu} and α_{Si} are in /°C. It is worth mentioning that the present study considers only the square array of TSVs. However, on the basis of previous studies on metal-ceramic composites, the effective thermal expansion response is insensitive to the shape and distribution of the discrete phase [10,15]. As a consequence, Eqs. (2)–(4) should provide a reasonable approximation for the effective in-plane CTE, as long as there is a uniform distribution of Cu TSVs in the Si chip.

It is worth emphasizing that, although the linear relation in Eq. (2) appears simple, it is not a premise but an outcome of this study. The present numerical analysis is not predicated upon any analytical model. While analytical theories for the effective CTE of fiber-reinforced composites exist [16,17], in these composites the fiber lengths are much greater than the fiber diameter and inter-fiber spacing, so they have no direct bearing with the current TSV structure. The present numerical study illustrates that, at least for the Cu/Si TSV system, a rule-of-mixtures type of relation is a good approximation (being more accurate with higher aspect ratios).

3.2. Internal stress and deformation fields

We now present representative stress and deformation fields resulting from the thermal mismatch between Si and Cu. It is noted that, in an actual TSV structure, there may be connecting pads, solder bumps, and/or underfill in direct contact with the "free surface." Complications of deformation due to these features are not considered in this study. The case of heating from 20 to 320 °C is examined. In addition, a cooling case from 320 to 20 °C, where 320 °C is treated as the stress-free temperature, is also considered. It is worth pointing out that various fabrication processes can result in different stress-free states in the TSV structure, and there has been a wide range of initial states, from room temperature to around 300 °C, assumed in prior numerical studies [5,7–9,18–24]. Attention here is devoted to a baseline understanding of mismatch induced effects from two opposite thermal loading histories. The contour plots presented correspond to the case of TSV area fraction of 0.05 and $\frac{h}{p} = 1.5$.

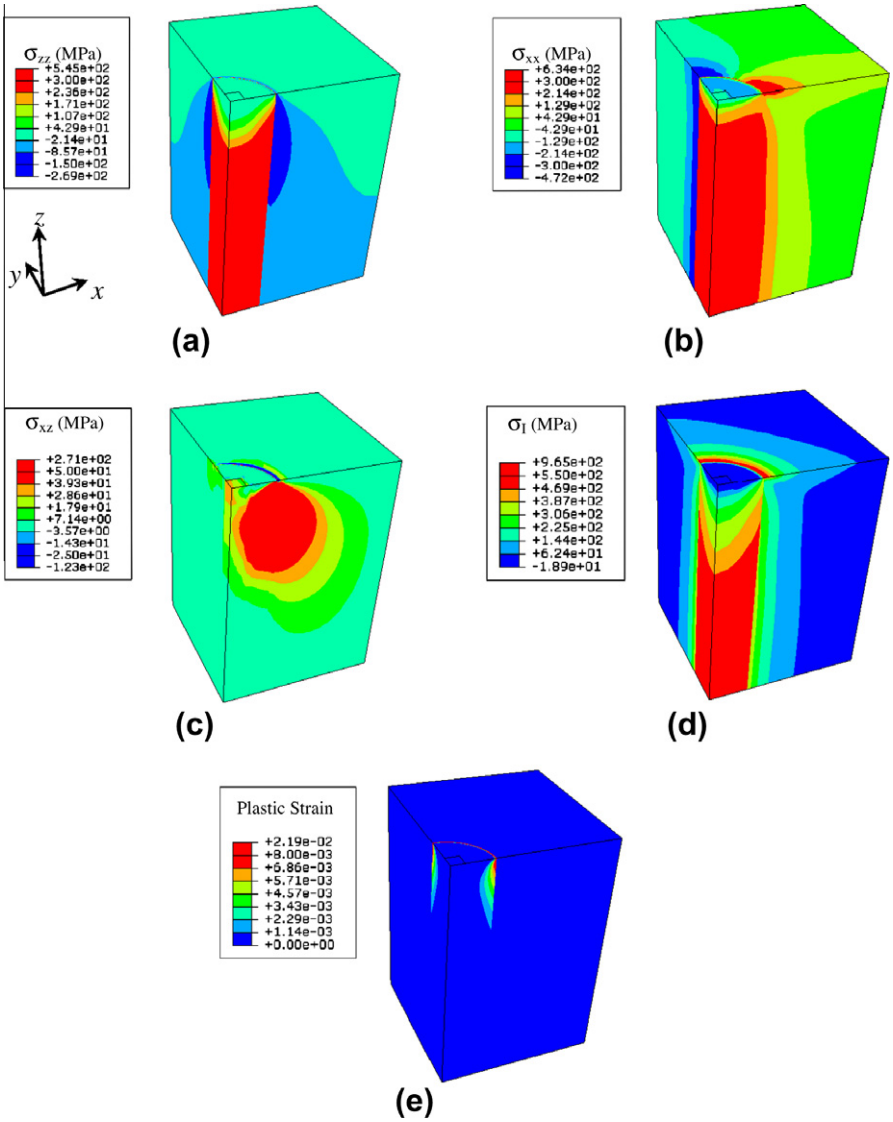

Fig. 6. Contour plots of (a) normal stress σ_{zz}, (b) normal stress σ_{xx}, (c) shear stress σ_{xz}, (d) maximum principal stress and (e) equivalent plastic strain, in the TSV structure with 0.05 area fraction of Cu and h/p = 1.5, after cooling from 320 to 20 °C.

Fig. 5a–e show the contour plots of stresses σ_{zz}, σ_{xx}, σ_{xz}, maximum principal stress, and equivalent plastic strain, respectively, upon heating from 20 to 320 °C. It can be seen that the Cu TSV is generally under compression (Fig. 5a, b and d), because of its higher CTE value compared to Si. At deeper locations the magnitude of longitudinal compressive stress in Cu, σ_{zz}, is well above 500 MPa. Near the free surface the stress magnitudes are reduced. Shear stress exists across the interface between Cu and Si, especially near the free surface where the σ_{xz} magnitude can reach beyond 200 MPa (Fig. 5c). Plastic deformation in Cu appears in the interface region near the free surface (Fig. 5e), which raises concern for interfacial damage in the TSV structure.

Fig. 6 shows a similar set of contour plots, but for a thermal history of cooling from 320 to 20 °C. It can be seen that the Cu line is generally under tension after cooling (Fig. 6a, b and d). Plastic deformation still occurs in the interface region near the free surface (Fig. 6e), where the magnitudes of shear stress are also significant (Fig. 6c). At the same location across the interface, significant tensile stresses also exist (Fig. 6b). As a consequence, the risk of delamination damage is higher after cooling compared to the case of heating. The same results can also be viewed from the standpoint of residual stresses, because Fig. 5 (heating) and Fig. 6 (cooling) correspond to the cases, respectively, without and with thermal residual stresses at room temperature for the composite system. When the stress-free temperature is high, delamination may simply be induced by the residual stress at room temperature. This tendency is seen to be higher compared to the case of heating (over the same temperature span) when there is no starting stress at room temperature.

Although the temperature range considered for heating and cooling is the same, it is worth pointing out that the stress field after cooling (Fig. 6) is not the exact opposite of that after heating (Fig. 5) with the same magnitudes. This is due to the fact that plastic deformation in Cu occurs during the process, and the material properties used in the current modeling (including the yield strength and strain hardening of Cu) are functions of temperature. Naturally the extents of deformation and associated stress fields for heating and cooling should not be the same.

The stress field inside Si also deserves attention, since a high tensile stress increases the propensity of brittle fracture. Additionally, in TSV structures containing active devices, the presence of stresses can significantly affect carrier mobility [5]. From Figs. 5 and 6 the stress magnitudes in Si are greatest adjacent to the Cu TSV. The longitudinal component (σ_{zz}) in Si is generally of opposite sign to that in Cu. The lateral components in Si, however, can be in tension or compression depending on the location and orientation. It is noticeable, from Figs. 5d and 6d, that the maximum principal stresses in Si near the Cu line after heating and cooling are both in tension. The reason is that different stress orientations contribute to the principal component. In the case of heating, the high tensile principal stress is primarily due to the high tensile component along the circumferential direction right outside the cylindrical TSV. In the case of cooling, the maximum principal stress is most influenced by the high tensile radial component.

When taking into account the other geometric factors considered in this study, we found that the maximum shear stress at the interface decreases with increasing TSV area fraction. The same trend is also true for the maximum equivalent plastic strain. For example, with $\frac{h}{p} = 1.5$ the maximum shear stress magnitude decreases from 295 to 202 MPa when the TSV area fraction increases from 0.05 to 0.2 during heating from 20 to 320 °C; the corresponding decrease in maximum equivalent plastic strain is from 0.05 to 0.0344. This is primarily caused by the different ability of Cu near the free surface to overcome the surrounding constraint and expand/contract in the vertical (z) direction. For a wide TSV (higher area fraction), the near-surface Cu material has a greater freedom to change dimension in z so the constraint from Si will be reduced, and hence the smaller shear stress generated along the interface. Since plastic deformation is dictated by the deviatoric stress, it follows essentially the same trend as the shear component. The finding suggests that, within the present modeling framework, a TSV structure with a higher Cu content will be more beneficial for resisting delamination damage. The model height plays a relatively minor role in affecting this result.

4. Conclusions

Three-dimensional finite element analyses were carried out to study the effective CTE and thermal mismatch-induced deformation fields, in the Cu TSV-containing Si structure used for 3D microelectronic packaging applications. Salient findings are summarized in the following:

1. With a uniform distribution of the TSVs, the effective CTE increases nearly linearly with the area fraction of TSV. The temperature range used for determining the effective CTE also affects the result.
2. Quantification of the effective CTE values obtained from the present study (namely Eqs. (2)–(4)), can be used as model input in numerical modeling of larger 3D packaging structures if the TSV-containing Si chip is to be treated as a homogeneous material.
3. With the 300°C temperature difference considered, plastic deformation in Cu readily occurs, especially near the interface region close to the free surface. This, in conjunction with the high local shear stress in the same region, may cause delamination between the TSV and Si matrix. The same concern is greater in the case of cooling, because local tensile stresses also exist normal to the interface.
4. The maximum principal stress in Si adjacent to the TSV is tensile, with significant magnitudes, in both the cases of heating and cooling.
5. In general, the risk for delamination damage is smaller if the structure contains more densely distributed TSVs.

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