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Effects of TSVs (through-silicon vias) on thermal performances of 3D IC integration system-in-package (SiP)

John H. Lau [a,*], Tang Gong Yue [b]

[a] Electronics & Optoelectronics Laboratories, Industrial Technology Research Institute (ITRI), Chutung, Hsinchu 310, Taiwan, ROC
[b] United Test and Assembly Center (UTAC), 5 Serangoon North Ave. 5, Singapore 554916, Singapore

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ABSTRACT

Thermal performances of 3D IC integration system-in-package (SiP) with TSV (through silicon via) interposer/chip are investigated based on heat-transfer and CFD (computational fluid dynamic) analyses. Emphases are placed on the determination of (1) the equivalent thermal conductivity of interposers/chips with various copper-filled, aluminum-filled, and polymer w/o filler filled TSV diameters, pitches, and aspect ratios, (2) the junction temperature and thermal resistance of 3D IC SiP with various TSV interposers, (3) the junction temperature and thermal resistance of 3D stacking of up to 8 TSV memory chips, and (4) the effect of thickness of the TSV chip on its hot spot temperature. Useful design charts and guidelines are provided for engineering practice convenient.

1. Introduction

Moore's law (emphasizes on minimum costs and innovations) has been the most powerful driver for the development of the microelectronic industry. This law focuses on lithography scaling and integration (in 2D) of all functions on a single chip, perhaps through system-on-chip (SoC). On the other hand, the integration of all these functions can be achieved through system-in-package (SiP) or, ultimately, 3D IC integration SiP.

There are many critical issues of 3D IC integration [1–30], e.g., EDA (electronic design automation) softwares are not commonly available; test methods and equipments are lacking; known-good-die (KGD) are required; fast chips mixed with slow chips; large chips mixed with small chips; microbumps usually are required; equipment accuracy for alignments; wafer thinning and thin wafer handling during processes; thermal management issues; 3D inspection issues; 3D expertises, infrastructure, and standards are lacking; TSVs usually are required for 3D IC integration; TSV cost is higher than wirebonding; TSV high-volume production tools are lacking/expensive; TSV design guidelines are not commonly available; TSV design softwares are lacking; TSV technology usually requires microbumps; test methodology and softwares of TSV are lacking; copper filling helps on thermal but increases TCE (thermal coefficient of expansion); copper filling takes a long time (low throughputs); the tough requirements of TSV wafer yields (>99.9%); TSV wafer warpage due to TCE mismatch; thin TSV wafer handling during all the processes; TSV with high aspect ratios are difficult to manufacture at high yield; TSV inspection methodology; TSV expertises, infrastructure, and standards are lacking.

Fig. 1 shows the generic 3D technology roadmap for high-performance computing systems given by IBM [1]. It can be seen that in the next few year, TSV is used to stack up chips such as memories and TSV interposer is needed for supporting high-performance chips. The key function of this TSV interposer is to fan-out the very fine-pitch and high pin-count pads (circuitries) of the high performance chips with redistribution layers either on the top or bottom or both of the TSV interposer.

As mentioned, thermal management is one of the critical issues of 3D IC integration. This is because: (1) the heat flux generated by stacked multifunctional chips in miniature packages is extremely high; (2) 3D circuits increase total power generated per unit surface area; (3) chips in the 3D stack may be overheated if cooling is not properly and adequately provided; (4) the space between the 3D stack may be too small for cooling channels (i.e., no gap for fluid flow); and (5) thin chips may create extreme conditions for on-chip hot spots. Thus low-cost and effective thermal management design guidelines and solutions are desperately needed for widespread use of 3D IC integration SiP.

In this study, based on the theory of heat transfer, the thermal performances of high-performance packages with TSV interposers and memory chip stacking are studies. The results are plotted in useful design charts for engineering practice convenient and design guidelines are also provided.

Even with the most advanced softwares and high-speed hardwares, it is impossible to model all the TSVs in a 3D IC integration SiP. In this study, equivalent thermal conductivity of a TSV interposer/chip with various TSV diameters, pitches, and aspect ratios

* Corresponding author. Tel.: +886 3591 3390.
E-mail addresses: johnlau@itri.org.tw (J.H. Lau), gy_tang@sg.utacgroup.com (T.G. Yue).

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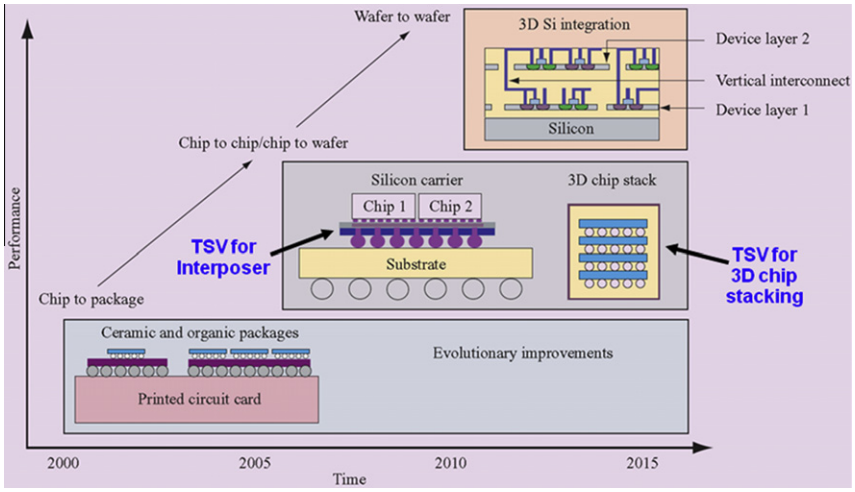

Fig. 1. IBM's generic 3D technology roadmap for high-performance computing systems.

(as shown in Fig. 2) are developed first through detailed 3D heat transfer and CFD analyses [31–34]. These equivalent thermal conductivities are then used (with the TSV chip/interposer as a block) to perform all the simulations reported herein.

2. Equivalent thermal conductivity of TSV interposers/chips

2.1. Methodology for extracting $k_{eq,z}$ and $k_{eq,x} = k_{eq,y}$

The TSV chip/interposer is schematically shown in the upper portion of Fig. 3. It can be seen that, unlike the thermal conductive of the ordinary silicon chip which is isotropic, because of the copper-filled TSVs, the thermal conductive of TSV silicon chip is anisotropic, i.e., the thermal conductivity in the *xy*-planar directions ($k_{eq,x} = k_{eq,y}$) is not equal to that in *z*-normal direction ($k_{eq,z}$).

The approaches for extracting ($k_{eq,z}$) and ($k_{eq,x} = k_{eq,y}$) are shown, respectively in the lower portion of Fig. 3. Firstly, construct the geometry of the copper-filled TSV chip with various diameters, pitches, and aspect ratios. Then, input the thermal material properties (Table 1) of all the elements in the model. Finally, apply the kinetic and kinematic boundary conditions and calculate the temperature distributions. The equivalent thermal conductivity can be obtained with the equations shown below.

$$q = -k_{eq,z}\frac{dT}{dz} = k_{eq,z}\frac{|\Delta T|}{\Delta z} \Rightarrow k_{eq,z} = q\frac{\Delta z}{|\Delta T|} \tag{1}$$

$$q = -k_{eq,x}\frac{dT}{dx} = k_{eq,x}\frac{|\Delta T|}{\Delta x} \Rightarrow k_{eq,x} = q\frac{\Delta x}{|\Delta T|} \tag{2}$$

$$k_{eq,y} = k_{eq,x} \tag{3}$$

For example, to extract the equivalent thermal conductivity in the *z*-direction, the geometry of the TSV chip is constructed, then a uniform heat flux (q) is imposed on the top surface of the TSV chip, and the bottom surface is set as isotherm boundary (25 °C), while the four-side surrounding boundaries are set as adiabatic boundaries.

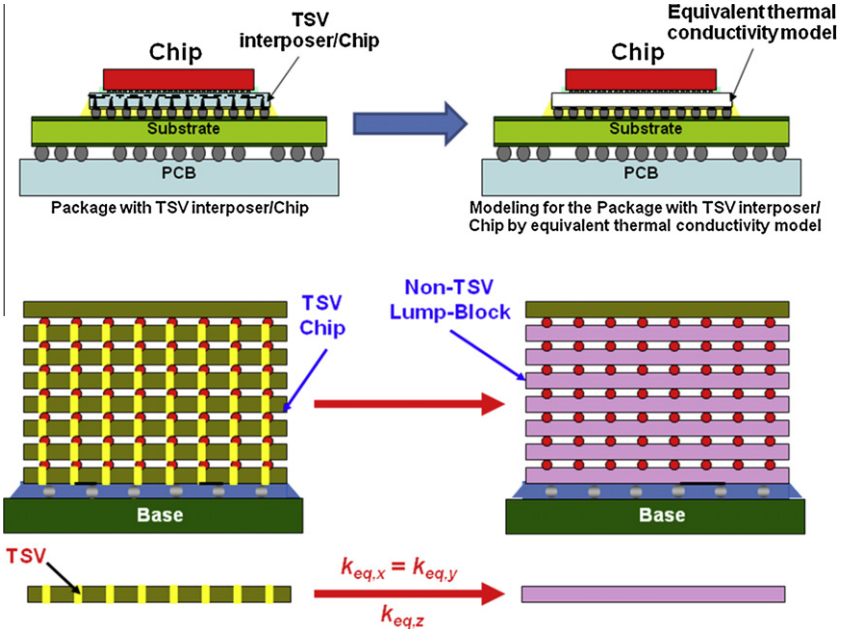

Fig. 2. Equivalent thermal conductivity model for TSV interposer/chip in a SiP for thermal analysis (each TSV interposer/chip as a lumped block).

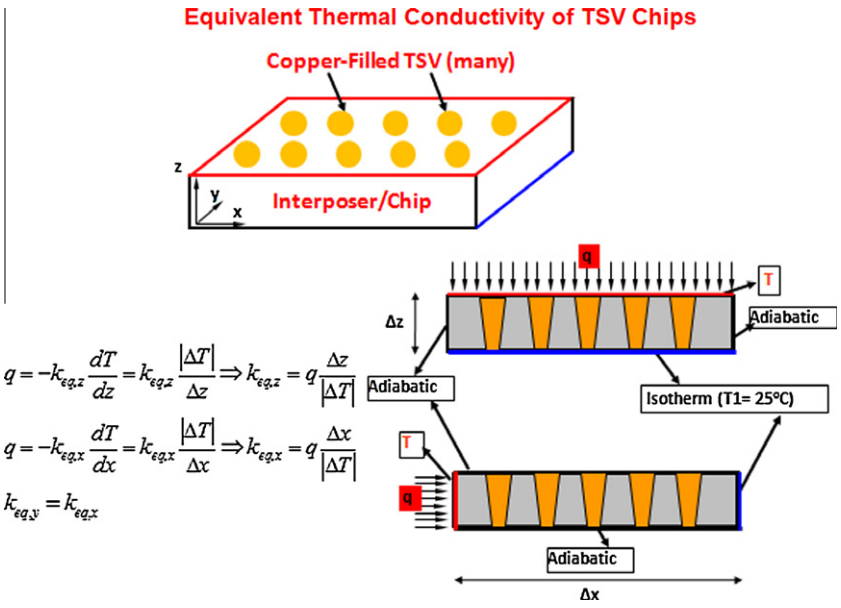

Fig. 3. Equivalent thermal conductivity extraction models for TSV interposer/chip.

Table 1
Geometry and thermal conductivity of materials for TSV interposer/chip.

Component	Interposer	TSV	TSV filler			
Material	Silicon	Copper	Polymer with filler particles	Polymer with filler particles	Al	Copper
Thermal conductivity (W/m°C)	150	390	4.0	25	237	390
Dimension detail (mm)	1.4 × 1.4 × 0.3	Varied	Copper plating thickness for partial filled via (5–25 μm)			
TSV pitch (mm)			0.15–0.6			

By using the Flowtherm software, the average temperature on the top surface of the TSV chip can be calculated and consequently ($k_{eq,z}$) can be obtained by Eq. (1). The geometries and thermal properties used for detailed modeling are listed in Table 1.

2.2. Effect of Cu-filled TSV diameter and aspect ratio on the equivalent thermal conductivity of TSV interposer/chip

Fig. 4 shows 5 different TSVs with different aspect ratios (A), which is defined as A = *Depth (0.3 mm)/Average diameter of TSV*. The thickness of the wafer is 300 μm and the etching angle of the tapered Cu-filled TSV is 85°. Figs. 5 and 6, respectively show the equivalent thermal conductivity of the TSV interposer/chip varies with TSV aspect ratio for equivalent thermal conductivity in the normal direction (z-direction), $k_{eq,z}$, and equivalent thermal conductivity in the planar directions (x and y-direction), $k_{eq,x} = k_{eq,y}$. It can be seen that (a) for a fixed pitch, the equivalent thermal conductivity of Cu-filled TSV interposer/chip increases when the aspect ratio decreases, which is especially sensitive when the aspect ratio is small – ranging from 2 to 4, and (b) the equivalent thermal conductivity in all directions is larger for larger diameters of the TSV. For engineering convenience, the results in Figs. 5 and 6 have been curve-fitted into the following empirical equations for the equivalent thermal conductivity

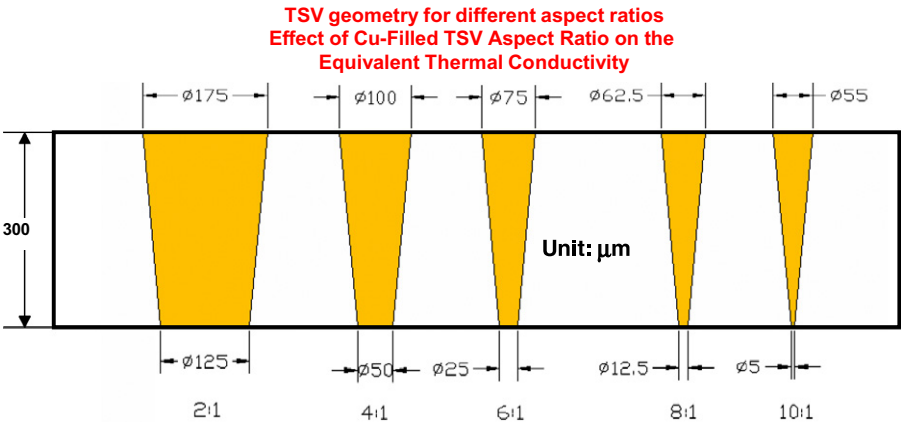

Fig. 4. TSV geometry for different aspect ratios.

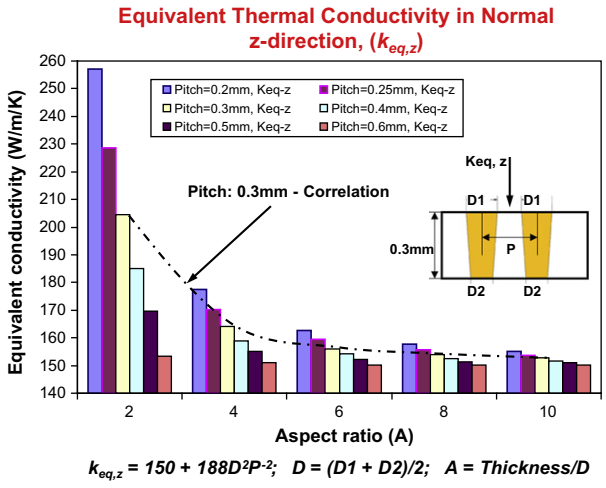

Fig. 5. Equivalent thermal conductivity in normal z-direction, ($k_{eq,z}$).

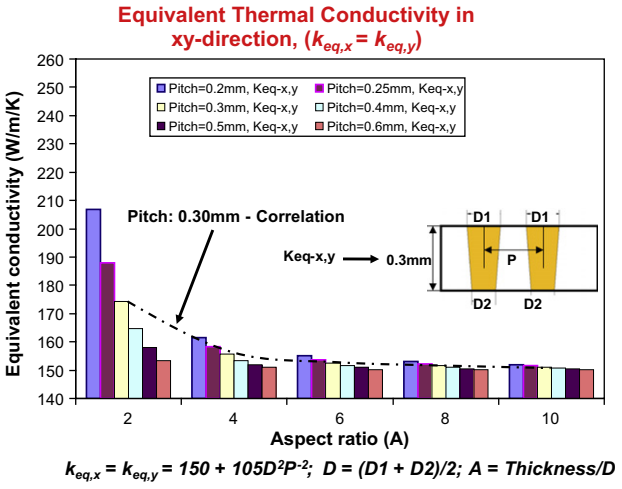

Fig. 6. Equivalent thermal conductivity in xy-direction, ($k_{eq,x} = k_{eq,y}$).

$$k_{eq,z} = 150 + 188D^2P^{-2}$$

$$k_{eq,x} = k_{eq,y} = 150 + 105D^2P^{-2}$$

where P is the pitch and $D = (D1 + D2)/2$ is the diameter and $D1$ and $D2$ are the diameters of a tapered TSV chip. The accuracy of these equations has been demonstrated by showing the correlation between the empirical equations (for the case of $P = 0.3$ mm) with the detailed 3D CFD analyses, as shown in Figs. 5 and 6. Consequently, these empirical equations will be used for the TSV chips as a lumped block without any vias for analysis of the 3D SiP.

2.3. Effect of Cu-filled TSV pitch on the equivalent thermal conductivity of TSV interposer/chip

Fig. 7 shows the effect of the Cu-filled TSV pitch on the equivalent thermal conductivity of the TSV interposer/chip with a thickness of 300 μm and an average diameter of 75 μm. It can be seen that: (1) the equivalent thermal conductivity of TSV interposer/chip increases when TSV pitch decreases; (2) the equivalent thermal conductivity is larger than that of the pure silicon material; (3) the equivalent thermal conductivity in the z-direction ($k_{eq,z}$) is larger than that in x and y-direction ($k_{eq,x}$ and $k_{eq,y}$), and (4) the equivalent thermal conductivity is more sensitive to the smaller TSV pitches.

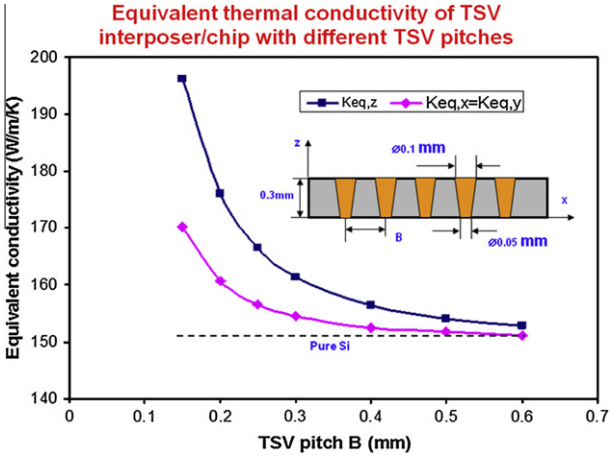

Fig. 7. Equivalent thermal conductivity of TSV interposer/chip with different TSV pitches.

2.4. Effect of plating thickness of partially Cu-filled TSV interposer/chip on their equivalent thermal conductivity

Fig. 8 shows a TSV with five different partially filled Cu thicknesses ($t = 5$ μm, $t = 10$ μm, $t = 15$ μm, $t = 20$ μm, and $t = 25$ μm). The wafer is 0.3 mm thick and there is no filler. It is assumed there is no free convection in the vias due to the tiny spaces. Figs. 9 and 10 show the variation of equivalent thermal conductivity of TSV interposer/chip with the partially plated copper thickness for different TSV pitch, respectively (a) in the normal direction (z-direction) and (b) in the planar directions (x and y-direction). It can be seen that equivalent thermal conductivities of the TSV interposer/chip increase with the plating thickness. In addition, the equivalent thermal conductivities of the TSV interposer/chip are more sensitive to the copper plating thickness for smaller pitches of vias. For example, in the case of 0.15 mm TSV pitch, the equivalent thermal conductivity in the z-direction increases from 138 W/m/K to 187 W/m/K (~40%) if the Cu plating thickness is increase from 5 μm to 25 μm. When the TSV pitch is 0.6 mm, then the equivalent thermal conductivity in the z-direction increases from 149 W/m/K to 153 W/m/K (less than 3%) if the Cu plating thickness is increase from 5 μm to 25 μm.

Why? Physically, the partially filled TSV consists of air and metal plating layer (i.e., copper). Since the thermal conductivity of air (0.026 W/m/K), copper (390 W/m/K) and silicon (150 W/m/K) is quite different, therefore various TSVs induce the variation of the thermal conductivity of the interposer/chip. For a given aspect ratio of TSV interposer/chip, the finer the TSV pitch the more the TSVs, and there is more copper or air but less silicon. Thus, the equivalent thermal conductivities of the TSV interposer/chip are more sensitive to the copper plating thickness for smaller pitches of TSV.

2.5. Effect of filler material of TSV interposer/chip on their equivalent thermal conductivity

Figs. 11 and 12 show the equivalent thermal conductivity of TSV interposer/chip with different filler materials, respectively (a) in the normal direction and (b) in the planar directions. The wafer is assumed to be 0.3 mm thick, the copper plating thickness is 10 μm, and the aspect ratio is 4. It can be seen that the overall trend is the equivalent thermal conductivity increases with the thermal conductivity of the filler materials. However, for the same reason as discussed in the previous section, the filler material has negligible effect on the equivalent thermal conductivity for TSV

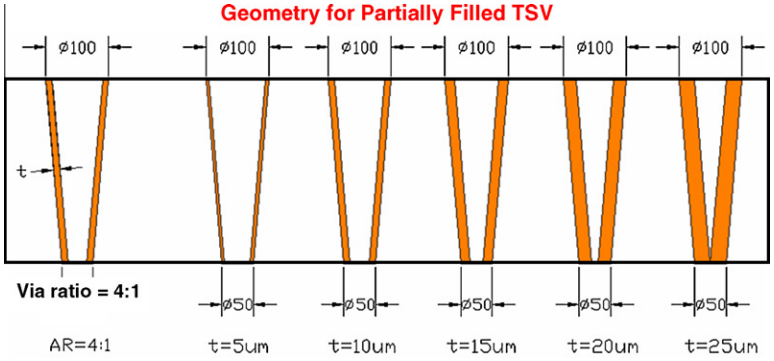

Fig. 8. Geometry for partially filled TSV.

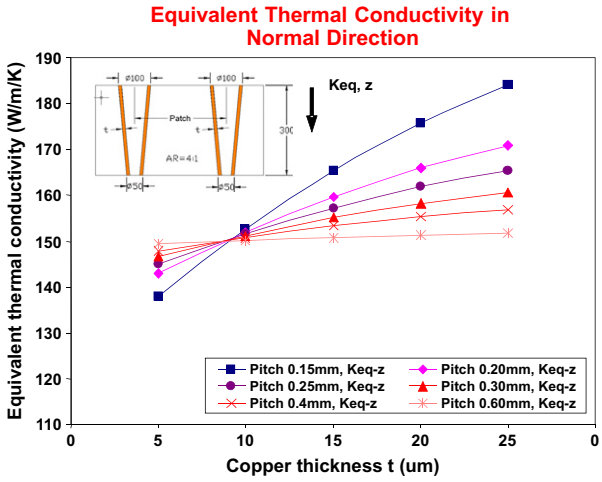

Fig. 9. Equivalent thermal conductivity ($k_{eq,z}$) for partially filled TSV.

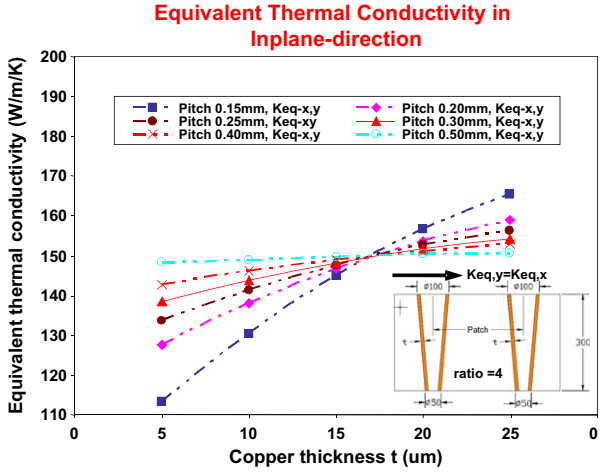

Fig. 10. Equivalent thermal conductivity ($k_{eq,x} = k_{eq,y}$) for partially filled TSV.

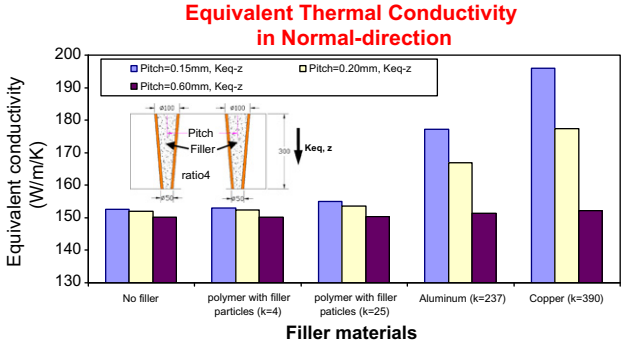

Fig. 11. Equivalent thermal conductivity ($k_{eq,z}$) of TSV with different filler materials.

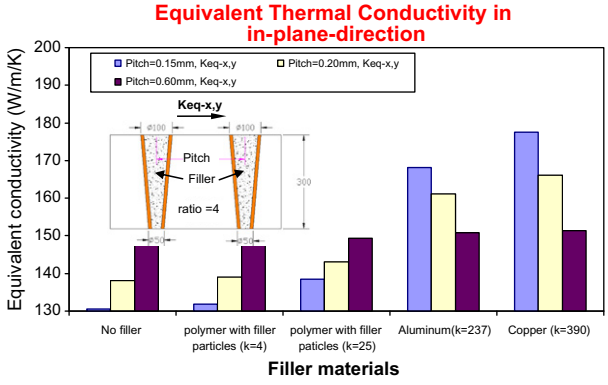

Fig. 12. Equivalent thermal conductivity ($k_{eq,x} = k_{eq,y}$) of TSV with different filler materials.

with larger pitches (e.g., pitch equals to 0.6 mm). Furthermore, it can be reveal that when the thermal conductivity of filler materials (e.g., 4 W/m/K and 25 W/m/K) is much less than that of the pure silicon interposer, the filler material has much larger effect on the equivalent thermal conductivity in the *x* and *y*-direction than that in the in *z*-direction. This is due to the thermal path in *x* or *y*-direction is partially isolated by the low thermally conductive material, while the thermal path smoothly goes through the silicon in the *z*-direction.

3. Effect of TSV interposer/chip on thermal performance of packages

3.1. Geometry and thermal properties of materials for package modeling

Fig. 13 shows the schematic for the compact modeling of the 3D SiP with the TSV chip/interposer which is modeled as a block (without TSV) with the determined equivalent thermal conductivities. This model consists of a large chip, a block (for the TSV interposer/

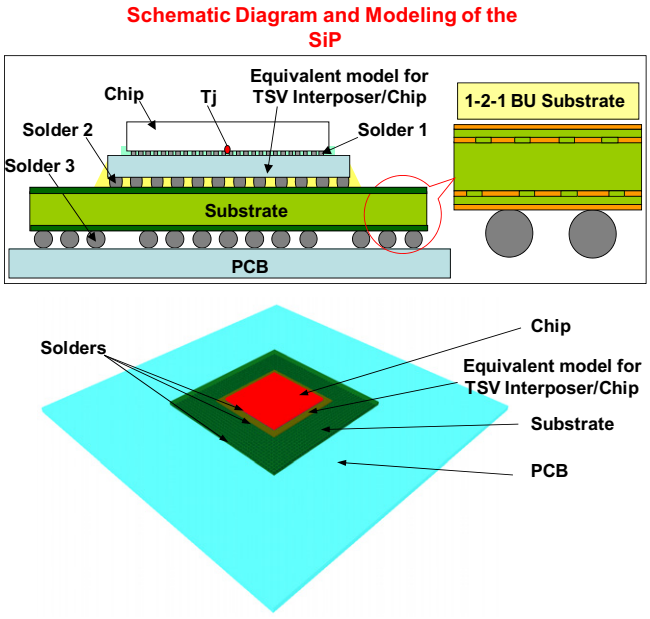

Fig. 13. Schematic diagram and modeling of the SiP.

chip), a 1-2-1 BU (build-up) substrate, a PCB, and solder joints. Their dimensions and thermal properties are listed in Table 2.

3.2. Effect of TSV interposer/chip on package thermal resistance

The junction to ambient thermal resistance of a package is often used as an index to describe the thermal performance of the package, the higher the thermal resistance the poor the thermal performance of the package. The junction to ambient thermal resistance of the package (R_{ja}) can be expressed as $R_{ja} = (T_j - T_a)/P$, where T_j and T_a respectively represent the junction temperature and ambient temperature, and P is total power dissipated from the chip.

3.2.1. Effect of chip power

Fig. 14 shows the junction to ambient thermal resistance of packages with different chip power dissipations. It can be seen that: (1) the thermal resistance reduces as the chip power increases (this is because high chip power induces high package temperature, as such high heat transfer coefficient is induced and more heat is removed from the package), and (2) the thermal resistance of the TSV package is lower than that of the package without TSV (this is because of the TSV interposer/chip's spreading effect). The dash lines in Fig. 14 represent the correlations between the thermal resistance and chip power when the junction temperature equals to 85 °C and 125 °C respectively.

3.2.2. Effect of interposer/chip size

Fig. 15 shows the effect of the TSV interposer/chip area on the package thermal performance. It can be seen that the thermal

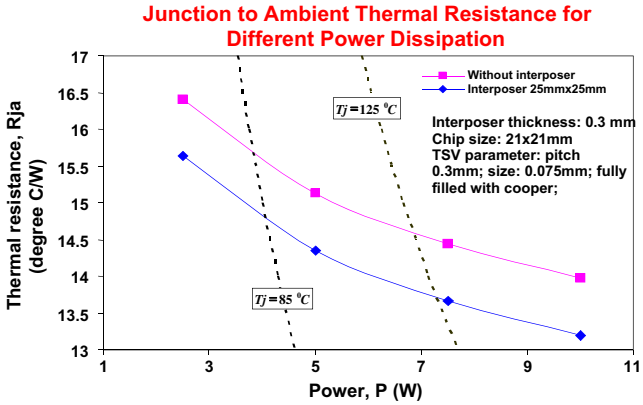

Fig. 14. Junction to ambient thermal resistance for different power dissipation.

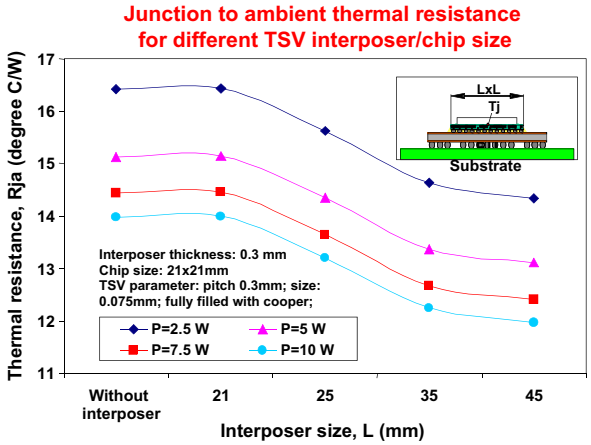

Fig. 15. Junction to ambient thermal resistance for different TSV interposer/chip size.

resistance (R_{ja}) decreases about 14% when the TSV interposer size increases from 21 × 21 mm to 45 × 45 mm. This indicates that package thermal performance can be improved by increasing the TSV interposer/chip size.

3.2.3. Effect of TSV interposer/chip thickness

Fig. 16 shows the effect of the TSV interposer/chip thickness on the package thermal performance. It can be seen that the thicker the TSV interposer/chip the lower the thermal resistance. This is because of the increasing spreading effect with thicker interposer/chip. However, for small size interposers, this effect is negligible.

3.2.4. Effect of high-performance chip size

Fig. 17 shows the effect of the chip size for different size ratios of the TSV interposer/chip to the chip on the thermal performance of the package. It can be seen that for the same size ratio of chip to

Table 2
Geometry and thermal conductivity of materials for the 3D IC SiP.

Component	Chip	Solder 1	Interposer	Solder 2	Substrate	Solder 3	PCB
Material	Si	SnAg	Si + TSV (Cu)	SnAg	Buildup	SnAg	FR4
Thermal conductivity (W/m/C)	150	57	k_{eq}	57	// 100 ⊥0.5	57	// 0.8 ⊥ 0.3
Dimension (mm)	21 × 21 0.75	Pitch: 0.15 Height: 0.08 Aver D: 0.08	Variable	Pitch: 0.5 Height: 0.1 Aver D: 0.1	1-2-1 (45 × 45 × 1)	Pitch: 1.0 Height: 0.6 Aver D: 0.6	101 × 114 × 1.6

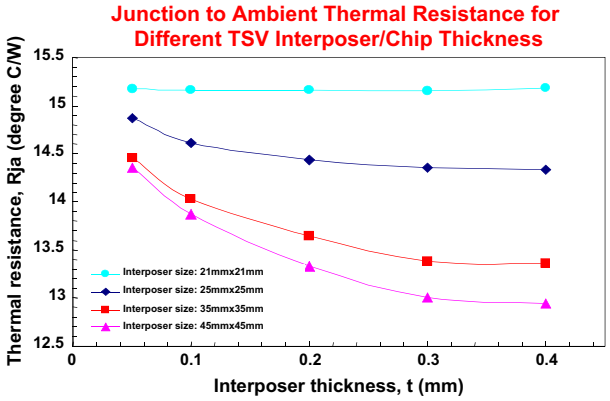

Fig. 16. Junction to ambient thermal resistance for different TSV interposer/chip thickness.

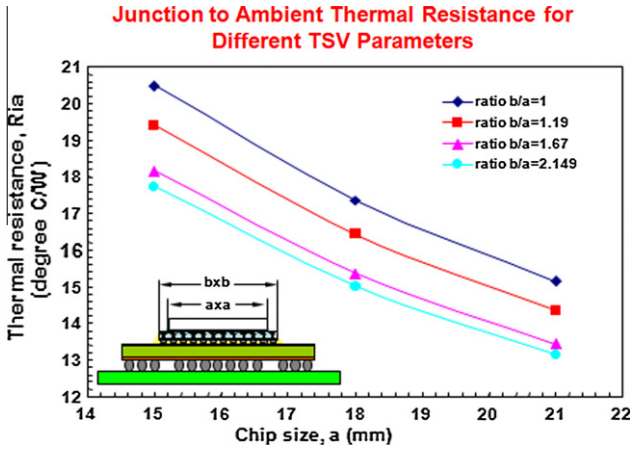

Fig. 17. Junction to ambient thermal resistance for different TSV parameters.

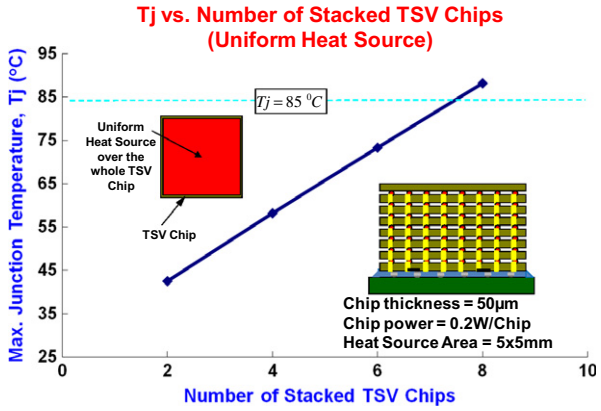

Fig. 18. T_j vs. Number of stacked TSV chips (uniform heat source).

TSV interposer/chip, the smaller sizes of chips induce higher thermal resistance of the package.

4. Thermal performance of 3D stacked TSV chips

4.1. Thermal performance of 3D stacked TSV chips with a uniform heat source

Fig. 18 shows the maximum junction temperature of a stacked chip (varying with the number of the chips) package. In these simulations, all the chips have the same size ($5 \times 5 \times 0.05$ mm), and there are 225 (15×15) copper-filled TSVs with a 0.2 mm pitch on each chip. The power dissipated by each chip is 0.2 W, and it is assumed that the power is uniformly distributed on each chip (Table 3). The ambient temperature is 25 °C. It can be seen from the figure that the maximum junction temperature increases linearly with the number of the chips stacked. In addition, it can be seen that if the maximum allowable junction temperature is 85 °C, then the maximum number of chips that can be stacked together is seven under the present conditions.

Fig. 19 shows the maximum junction temperature at each layer of the TSV chip stack. It can be seen that the maximum junction temperature difference between each layer of the stack is negligible. This means that the temperature distribution for the different

Table 3
Material properties for simulations.

	Chip	TSV	Bumps	Underfill	PCB
Material	Si (TSV)	Cu	SnAg	Polymer	FR4
k (W/m/°C)	Empirical equation	390	57	0.5	// 0.8 ⊥ 0.3
Dimension (mm)	5×5	∅ 0.05	∅ 0.20 Height = 0.15	$5 \times 5 \times 0.15$	$76 \times 114 \times 1.6$
Power (W)	0.2 W	N.A	N.A	N.A	N.A

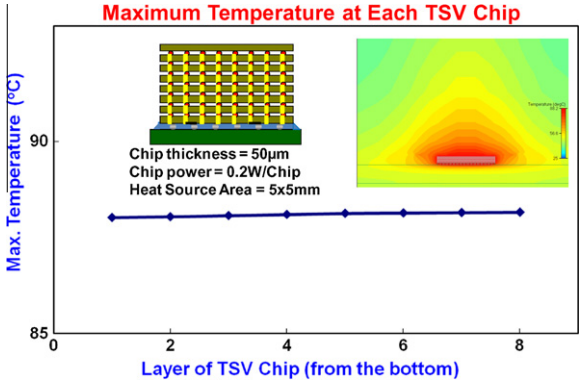

Fig. 19. Maximum temperature at each TSV chip.

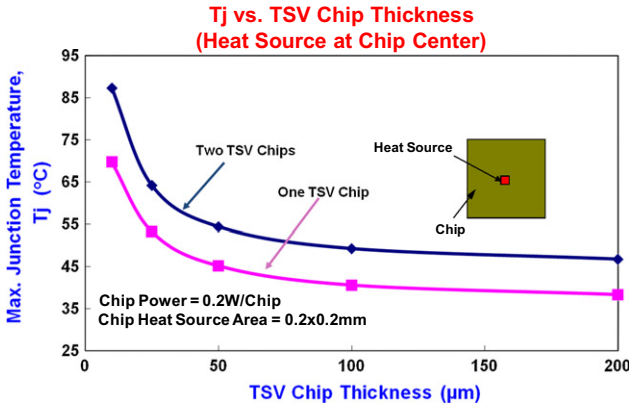

Fig. 20. T_j vs. TSV chip thickness (heat source at chip center).

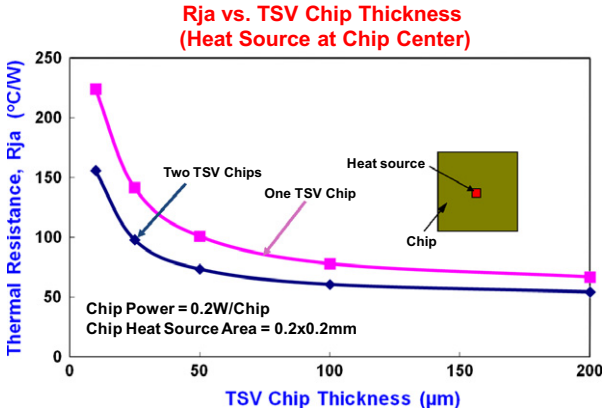

Fig. 21. R_{ja} vs. TSV chip thickness (heat source at chip center).

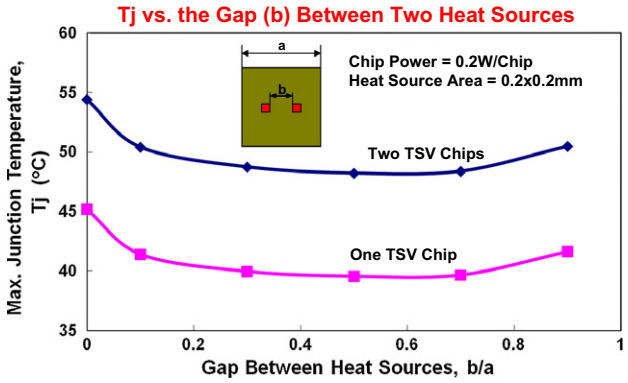

Fig. 22. T_j vs. the gap (b) between two heat sources.

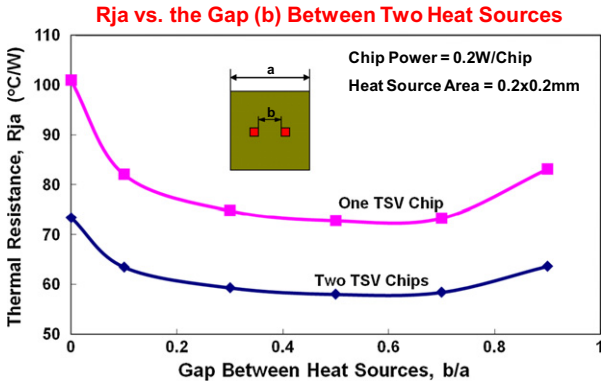

Fig. 23. R_{ja} vs. the gap (b) between two heat sources.

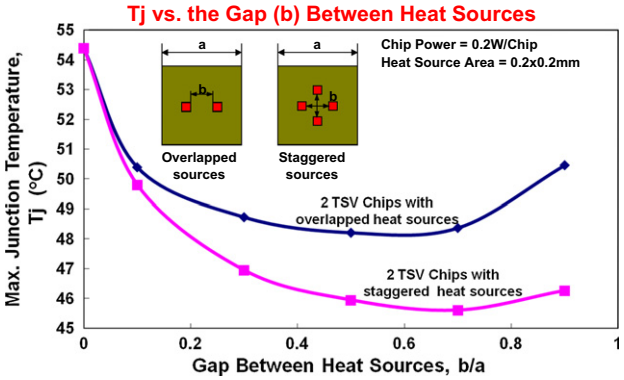

Fig. 24. T_j vs. the gap (b) between heat sources.

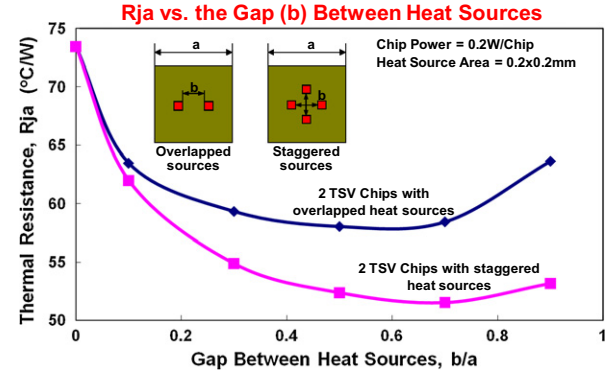

Fig. 25. R_{ja} vs. the gap (b) between heat sources.

layer of chips is uniform because we assumed that the power dissipation is uniformly distributed in each chip.

4.2. Thermal performance of 3D stacked TSV chips with a nonuniform heat source

The results presented in Figs. 18 and 19 are based on the assumption that the power is dissipated uniformly over the whole chip. However, in most applications, the power dissipated by each chip is basically nonuniform, and as such, it will induce quite different thermal behaviors of the 3D IC stack with TSV chips. In addition, it is well known that ordinary silicon chips normally have large parallel conduction of heat (parallel to the chip surface) owing to the large thermal conductivity of the Si material. However, for 3D IC chip stacking, in order to have a low profile, the chip thickness of each layer of the 3D stack must be ground down to 50 μm and less. Thus the parallel spreading effect is suppressed by the very thin chip, and the hot spot will be very intense. Compounding this with the nonuniform heat source it becomes a challenge in 3D IC integration stack.

4.2.1. Two TSV chips (each with one distinct heat source)

Figs. 20 and 21 show the thermal performance of a 3D integration of two copper-filled TSV chips stacking. All the chips are 5 mm × 5 mm and each chip's center is subjected to a distinct heat source (0.2 W) in a tiny area (0.2 × 02 mm). It can be seen from Figs. 21 and 22 that (for both one- and two-chip stacks) (1) for a nonuniform heat source, the effect of chip thickness on the thermal performance of 3D IC integrations is very important, (2) this thickness effect is even more significant in the application range (⩽50 μm) of 3D IC integrations, and (3) the maximum junction temperature and thermal resistance decrease as chip thickness increases.

4.2.2. Two TSV chips (each with two distinct heat sources)

In addition to one heat source per chip (5 × 5 mm), Figs. 22 and 23 show the effect of two heat sources at a distance apart (gap) on the thermal performance of 3D IC integrations of copper-filled TSV chips. There are two distinct heat sources (each with 0.1 W and on 0.2 × 0.2 mm area) on each chip (5 × 5 × 0.05 mm). It can be seen from the figures that (1) the larger the gap ($b/a \leqslant 0.7$) between the two heat sources, the better is the thermal performance (i.e., lower

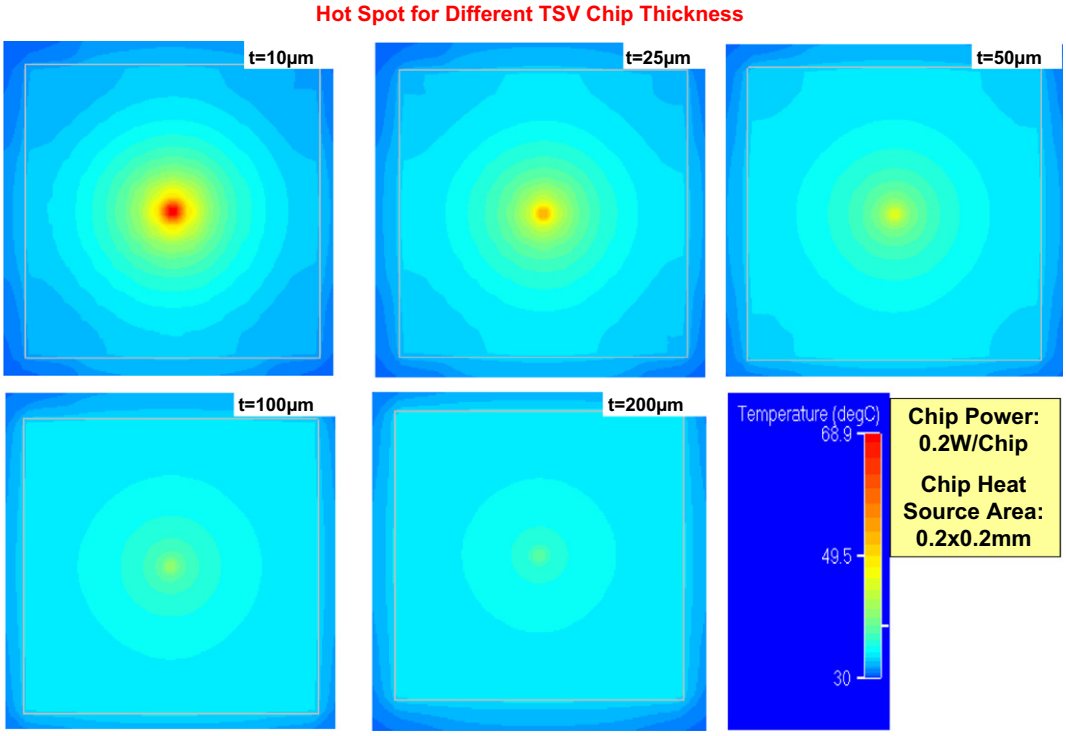

Fig. 26. Hot spot for different TSV chip thickness.

maximum junction temperature and thermal resistance), and (2) when the gap between the two heat sources is larger than 0.7 (i.e., the heat sources are too close to the edge of the chip), the thermal performance is weaker. This is due to suppressible spreading effects near the edges of the chips.

4.2.3. Two TSV chips with two staggered distinct heat sources

In addition to the case of overlapping heat sources discussed in the preceding paragraph, finally, Figs. 24 and 25 show the orientation effect (staggered heat sources) of two stacked chips, each with two heat sources at a certain distance apart, on the thermal performance of a 3D stack. It can be seen that (1) similar to case of overlapping heat sources, the larger the gap ($b/a \leqslant 0.7$) between those two pairs of staggered heat sources, the lower are the maximum junction temperature and thermal resistance, (2) when the gap between the two pairs of staggered heat sources is larger than 0.7 (i.e., the heat sources are too close to the edge of the chip), the thermal performance is weaker, and (3) the maximum junction temperature and thermal resistance of the 3D stack with two TSV chips subjected to two pairs of staggered heat sources are lower than those with two pairs of overlapping heat sources. This is so because the staggered heat sources avoid the superimposition of heat sources and thus lead to better thermal performance. This result is very useful for the design and layout 3D stack because it permits relocation of the heat sources and/or rotation of the chip.

4.3. Effect of thickness of the TSV chip on its hot spot temperature

Fig. 26 shows the temperature maps on a TSV chip with various chip thicknesses (10–200 μm). The chip is 5 mm × 5 mm and its center is subjected to a distinct heat source (0.2 W) in a tiny area (0.2 × 0.2 mm). It can be seen that the heat on the chip surface is well dissipated for typical chip thicknesses of 100–200 μm subjected to the generated power of 0.2 W. For the 200-μm-thick chip, the temperature distribution is almost uniform and equal to 35 °C. However, the hot-spot temperature on the chip increases to 69 °C (0.2 W powers) if the chip thickness is reduced to 10 μm and the hot-spot area is clearly shown. Thus, for a 0.4 W of powers (which is very common for DRAM) in a 5 mm × 5mm chip with 10 μm thickness, the hot-spot temperature could be 138 °C, which far exceeds the maximum allowable junction temperature (usually is 85 °C) of most Si chips.

5. Summary

In this study, the method used to extract the equivalent thermal conductivity of TSV interposer/chip has been established. Also, the equivalent thermal conductivity of interposer/chip with various TSV parameters has been extracted. Furthermore, modeling and simulation to determine the effects of TSV interposer/chip on the thermal performance of the 3D SiP have been conducted and presented. Some important results are summarized in the following.

- The accuracy of the proposed empirical equations for the equivalent thermal conductivity of copper-filled TSV chips has been demonstrated by correlated with the simulation results.
- The equivalent thermal conductivity of TSV interposer/chip can be increased by reducing the pitch and aspect ratio of the TSVs, as well as increasing the plating thickness of partial filled TSVs and using highly conductive filler materials.
- For the TSV interposer/chip under consideration, the equivalent thermal conductivity of the TSV interposer/chip is very sensitive to the TSV pitch ranging between 0.1 mm and 0.3 mm, and the aspect ratio ranging between 2 and 4.
- The finer the TSV pitch the more sensitive effects of the Cu plating thickness on the equivalent thermal conductivity.
- When the thermal conductivity of filler material is less than that of the pure silicon, the filler material has negligible effect on the equivalent thermal conductivity of the TSV interposer/chip in normal direction (z-direction).
- The TSV interposer/chip improves the thermal performance of the 3D SiP due to spreading effects.

- Junction to ambient thermal resistance of the SiP decreases 14% when the TSV interposer/chip size increased from 21 × 21 mm to 45 × 45 mm.
- Junction to ambient thermal resistance of the SiP decreases 11% when the TSV interposer/chip thickness increases from 50 μm to 400 μm.
- The larger the number of stacked TSV chips the higher the maximum junction temperature. Thus, the number of stacked chips is limited by the allowable thermal budgets.
- Chip thickness plays a very important role in thermal performance of 3D SiP. The thinner the chip the higher the maximum junction temperature and thermal resistance.
- For the present boundary conditions, the thinner the chip the more intensive the hot spot. When the chip thickness is 50 μm or less, the hot spot is very sensitive to the chip thickness.
- The larger the gap of distinguish pairs of overlapped heat sources on the 3D TSV chips the better the thermal performance, provided the pairs of heat sources are not near to the edges of the chip.
- The distinguish pairs of staggered heat sources on the 3D TSV chips lead to better thermal performance than the pair of overlapped heat sources.

Acknowledegments

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