ELEC-H-473 Microprocessor Architectures Words 'n shit

Glossary

AVX

Latest edition of SSE (2011).

IA-32

aka i386, third generation of x86 architecture, the first supporting 32-bits computing.

MMX

First SIMD introduced in 1997.

PGA

The package is square or rectangular, and the pins are arranged in a regular array on the underside of the package..

QFP

Surface mount integrated circuit package with "gull wing" leads extending from each of the four sides.

SSE

Evolution of MMX (1999).

Opcode

Code of the current instruction.

$\mathbf{X}\mathbf{M}\mathbf{M}$

 $128~{\rm bits}$ registers for Streaming SIMD Extension (SSE).

$\mathbf{Y}\mathbf{M}\mathbf{M}$

256 bits registers for Advanced Vector Extensions (AVX).

Acronyms

ACC

Accumulator.

ACPI

Advanced Configuration and Power Interface.

ALU

Arythmetic Logic Unit.

\mathbf{AVX}

Advanced Vector Extensions.

BTB

Branch Target Buffer.

\mathbf{BW}

Bandwidth.

CISC

Complex Instruction Set Computer.

Clk

Clock.

CMOS

Complementary Meta-Oxid-Semiconductor.

\mathbf{CPI}

Cycles Per Instruction.

CTRL

Control.

DDR

Double Data Rate.

\mathbf{DMI}

Direct Media Interface.

\mathbf{DRAM}

Dynamic Random Access Memory.

\mathbf{DSP}

Digital Signal Processing.

DTLB

Data Translation Lookaside Buffer.

DVFS

Dynamic Voltage and Frequency Scaling.

\mathbf{FF}

Flip-Flop.

FIFO

First In First Out.

FinFET

Fin-shaped Field Effect Transistor.

FIR

Finite Impulse Response.

\mathbf{FP}

Floating Point.

FPGA

Field-Programmable Grid Array.

\mathbf{FPU}

 ${\bf Floating\text{-}Point\ Unit.}$

GPP

General Purpose Processor.

GPR

General Purpose Register.

IA-32

Intel Architecture 32 bits.

IC

Instruction Count — Integrated Circuit.

ILP

Instruction-Level Parallelism.

IPC

Instructions Per Cycle.

\mathbf{IR}

Instruction Register.

ISA

Instruction Set Architecture.

ITLB

Instruction Translation Lookaside Buffer.

LEA

Load Effective Address.

\mathbf{LLC}

Least Level Cache, aka L3.

LRU

Least Recently Used.

LUT

Look-up Table.

MCP

Master Control Program.

MESI

Modified Exclusive Shared Invalid.

MIMD

Multiple Instruction Multiple Data.

MISD

Multiple Instruction Single Data.

MMX

MultiMedia eXtension.

MOSFET

Meta-Oxid-Semiconductor Field-Effect Transistor.

OSPM

Operating System-directed configuration and Power Management.

\mathbf{PC}

Program Counter.

PCH

Platform Controller Hub.

PGA

Pin Grid Array.

QFP

Quad Flat Package.

RAT

Register Alias Table.

\mathbf{RF}

Register File.

RISC

Reduced Instruction Set Computer.

SDRAM

Synchronous Dynamic Random Access Memory.

SIMD

 ${\bf Simple\ Instruction\ Multiple\ Data}.$

SISD

Single Instruction Single Data.

\mathbf{SMT}

Simultaneous MultiThreading, aka HyperThreading.

\mathbf{SoC}

System on Chip.

SRAM

Static Random Access Memory.

SSE

Streaming SIMD Extension.

\mathbf{STLB}

Shared Translation Lookaside Buffer.

TDP

Thermal Design Power.

WB

Write-back.