Chapter 7

VLSI Fabrication Technology

Outline

- Foundries
- Foundry operations
  - Si waffers
  - Etching
  - Photolitography
  - Adding new materials
  - Doping
- NMOS technology
  - Example: making a NMOS inverter
- CMOS technology

Foundries

IC foundry

- Foundry = factory of integrated circuits

- What is special?
  - physico-chemical processes
  - extremely pure materials (atomic-level)
  - very precise and high temperatures
  - below micrometer-level position control

- ex: Fab2 Mietec: 33.000 EUR/m2 (1993)

Foundries

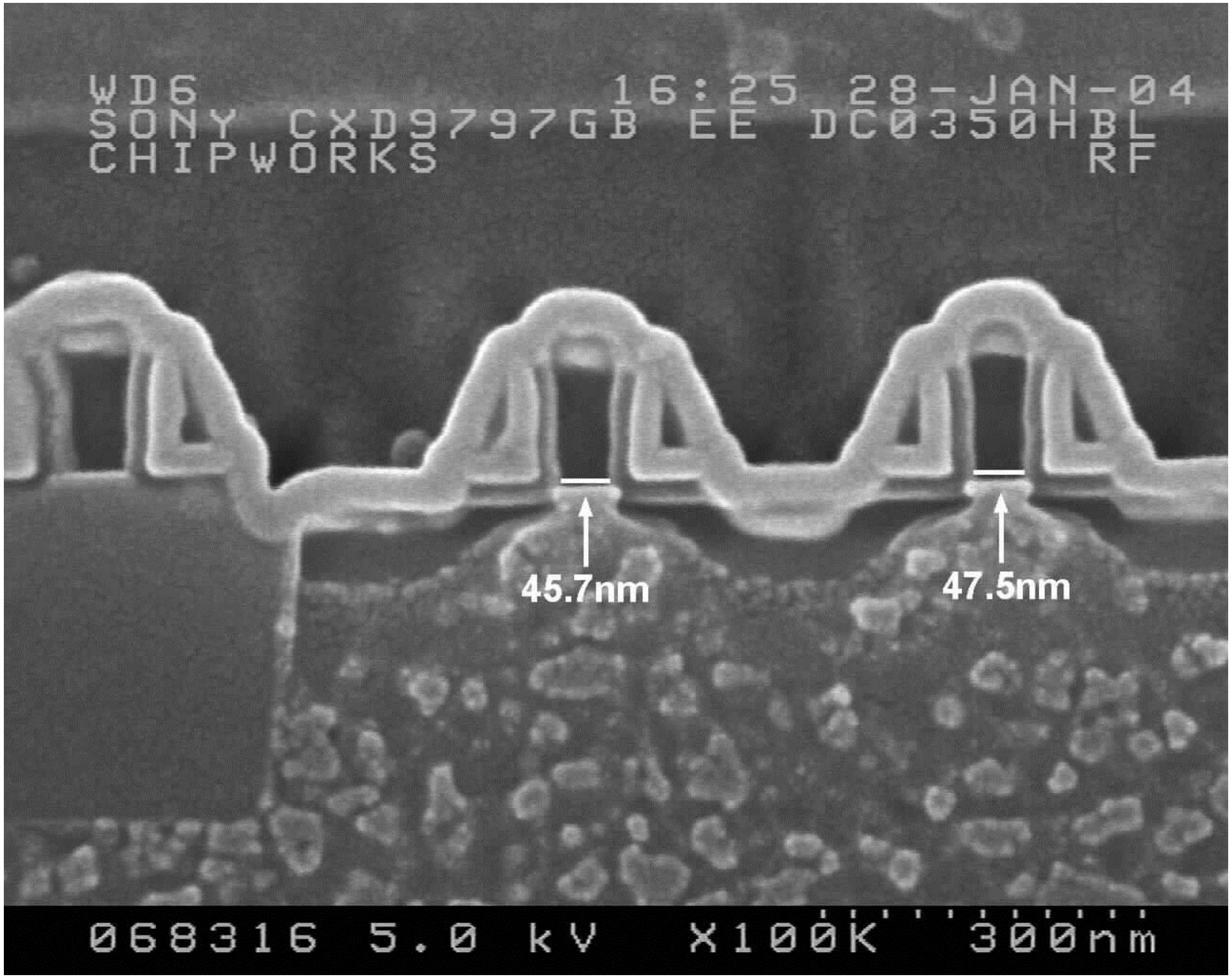
Clean room

- pollutants-"free" environment
  - dust
  - microbes
  - impurities, etc

- class 1: <1 particle of 0,1µm by foot^3
- hospital = class 10000

Foundry operations

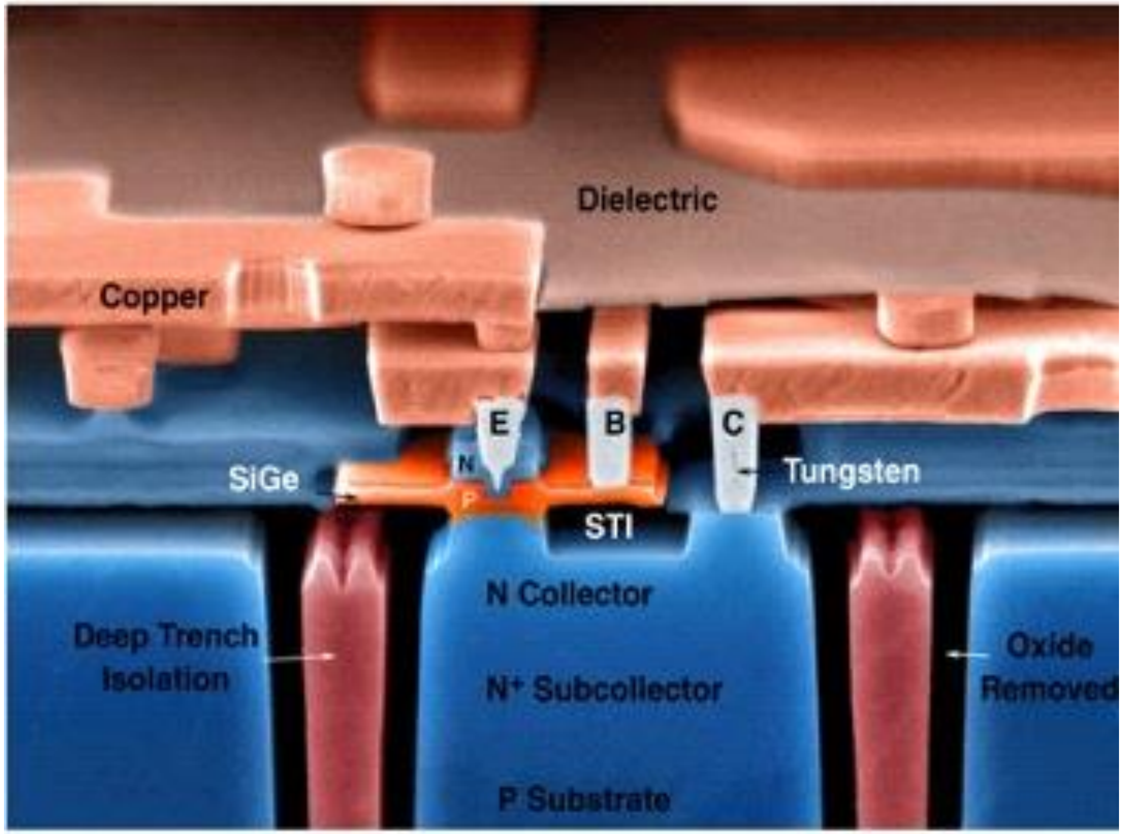
Chip = 3D structure at μm/nm scale



Foundry operations

Chip = 3D structure at μm/nm scale

- …obtained via successive 2D processes



Starting point: silicon wafers

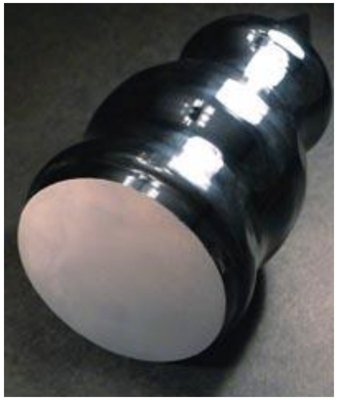
Preparing the substrate

- starting material : silica
- => MGS (metallurgical grade) silicon
  - impurities: about 10 ppm
- => EGS (electrical grade) silicon
  - Impurities << 0,002ppm

Starting point: silicon wafers

Preparing the substrate

- growth of a Si monocristal
- sawing
- oxidation (protection)



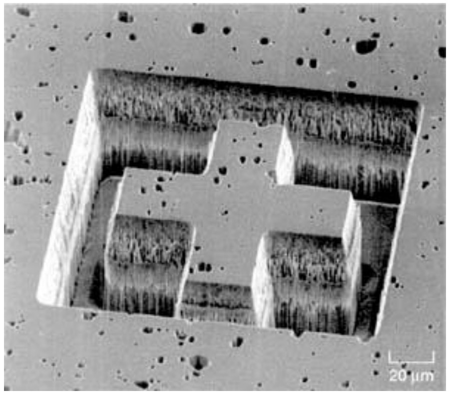
Starting point: silicon wafers

diameter: 5 to 50cm / thickness: 500µm

Foundry operations

Si wafer undergoes a set of physico-chemical processes

- engraving a pattern
  - photolithograpy + etching
- modifying electrical properties of Si
  - doping
- add new material
  - oxidation
  - epitaxy (cristal growth)
  - thin film deposition (chemical vapor deposition)
  - metallization

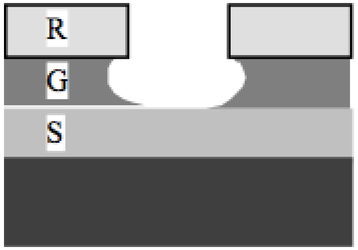


Engraving a pattern

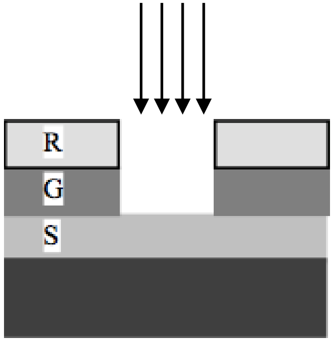
Etching

- Principle
  - remove material according to a given pattern
  - out-of-pattern zones protected by a film (resist)

- 1) chemical etching
  - chemical agent attacking Si
  - Drawback: isotropic attack



- 2) plasma etching
  - plasma = ionized gas (ions + free e^-)
  - physical + chemical attack
  - Anisotropic => better pattern



Engraving a pattern

Photolitography

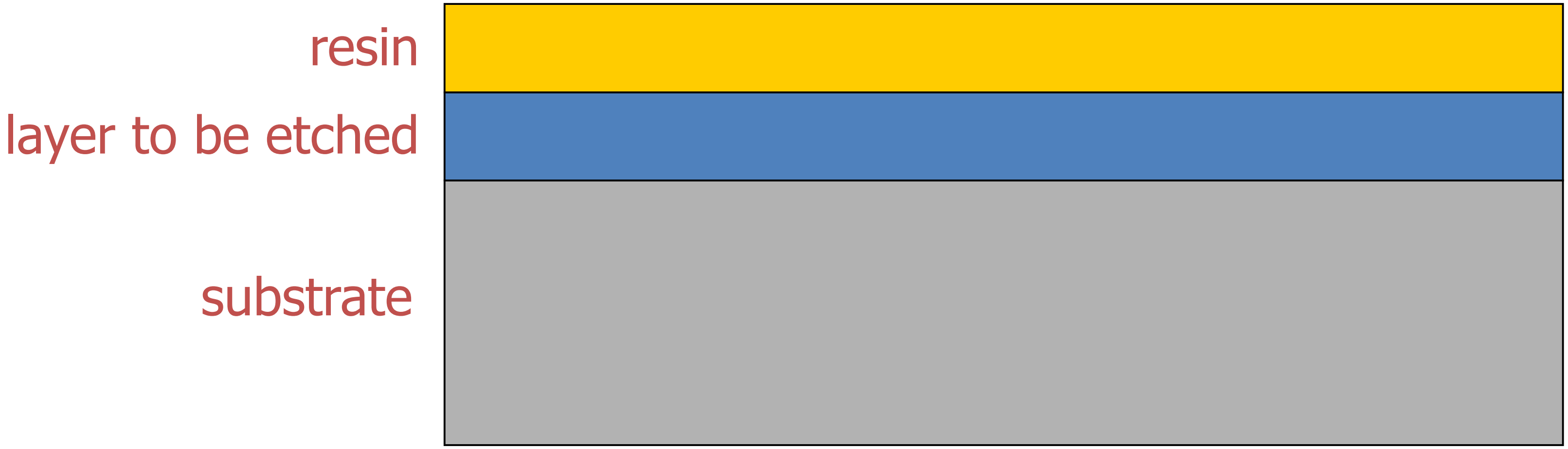
- Principle
  - laying down on the wafer a film of "resist" (resin) according to a given pattern, in order to peform a subsequent operation (etching, growth, etc)
  - used several times during the chip fabrication
- steps
  - 1) laying down a uniform film of resin
  - 2) exposure to UV through a mask => exposed regions of resin are chemically modified
  - 3) wafer cleaning => remove modified regions
  - 4) subsequent process (ex: etching)
  - 5) wafer cleaning => unmodified resin removal

Photolithography

0) starting situation

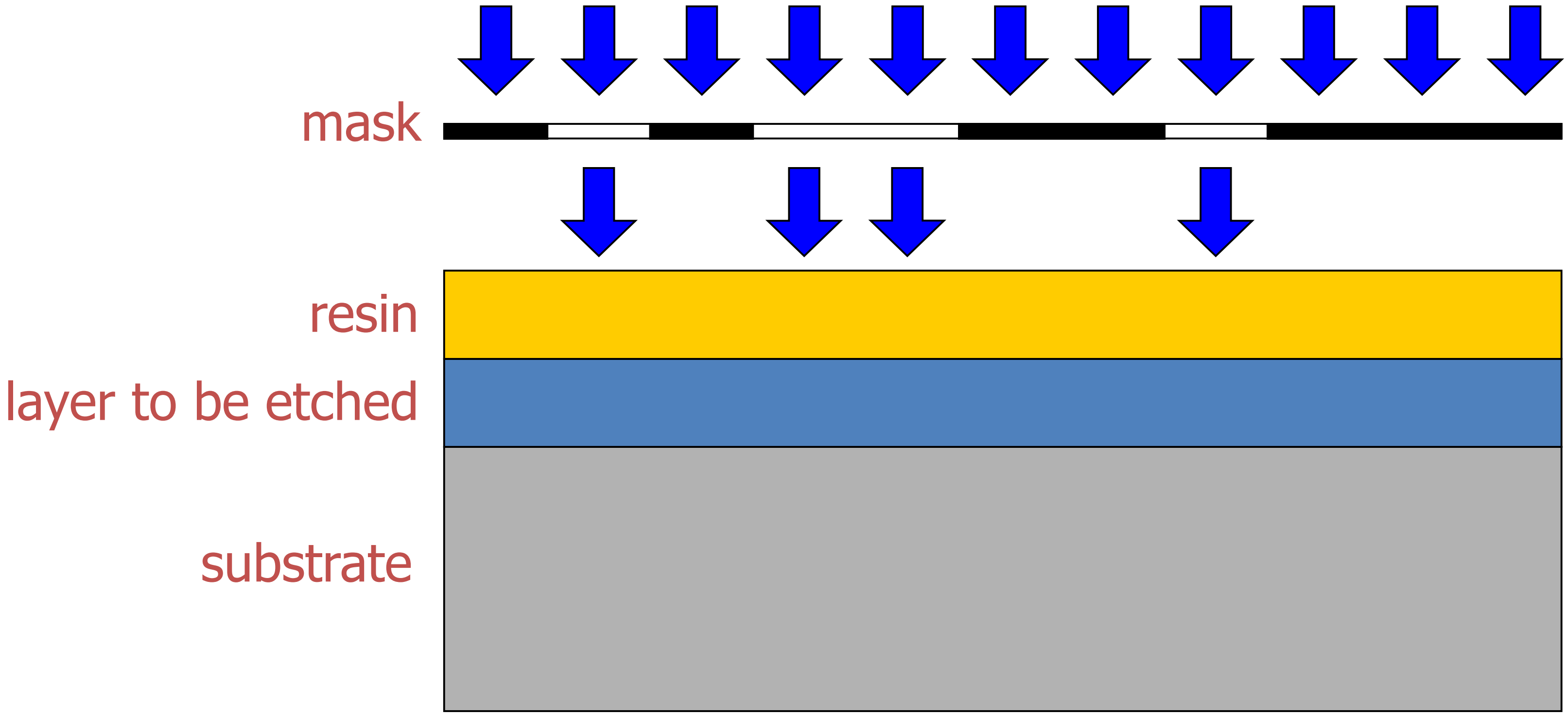
Photolithography

1) laying down a uniform layer of resin



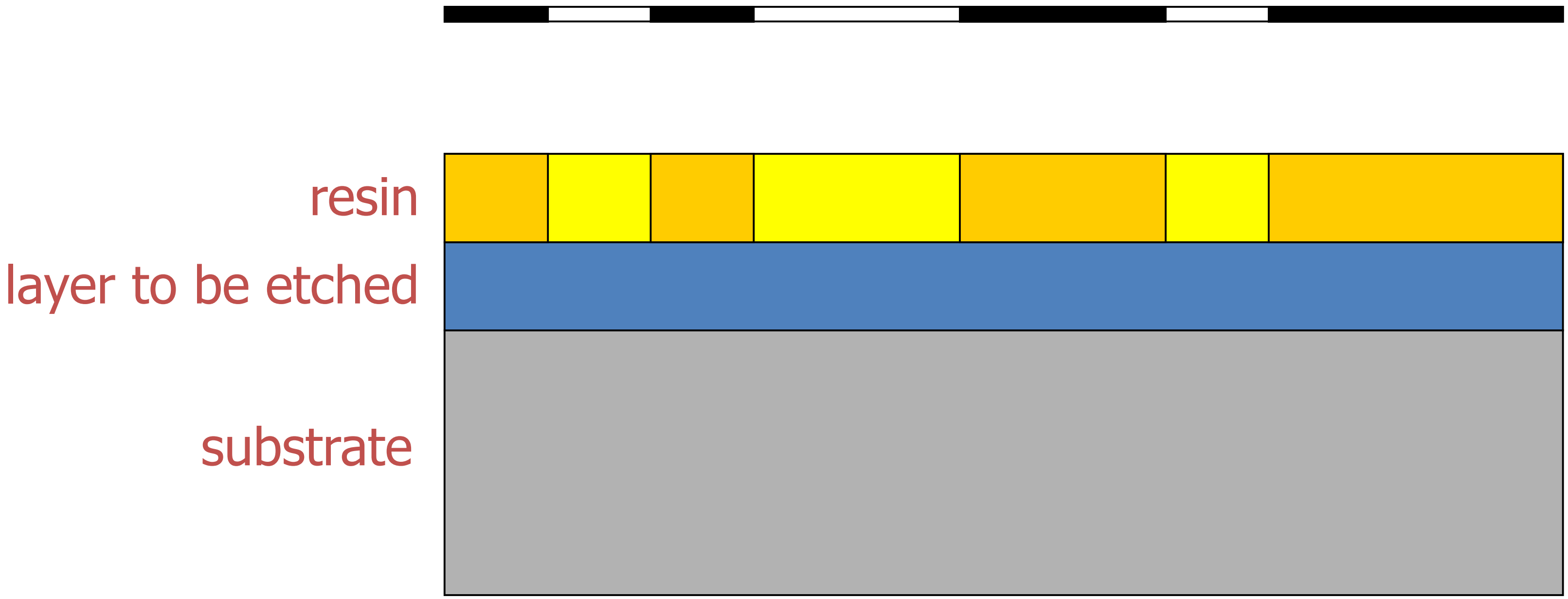
Photolithography

2) exposure through a mask



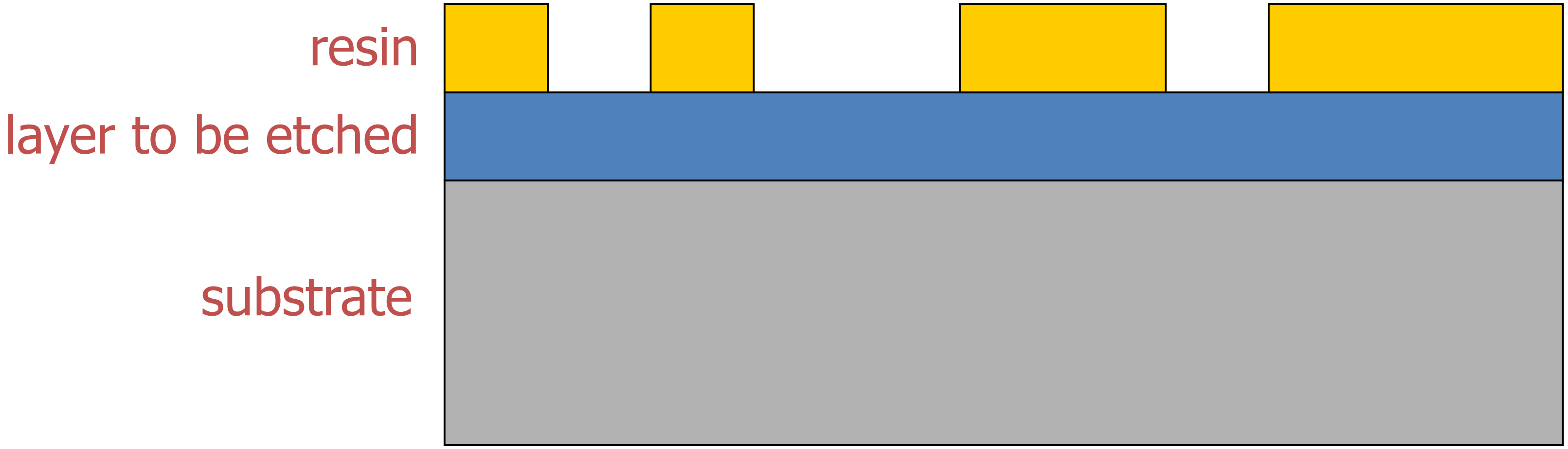
Photolithography

2) end of exposure:



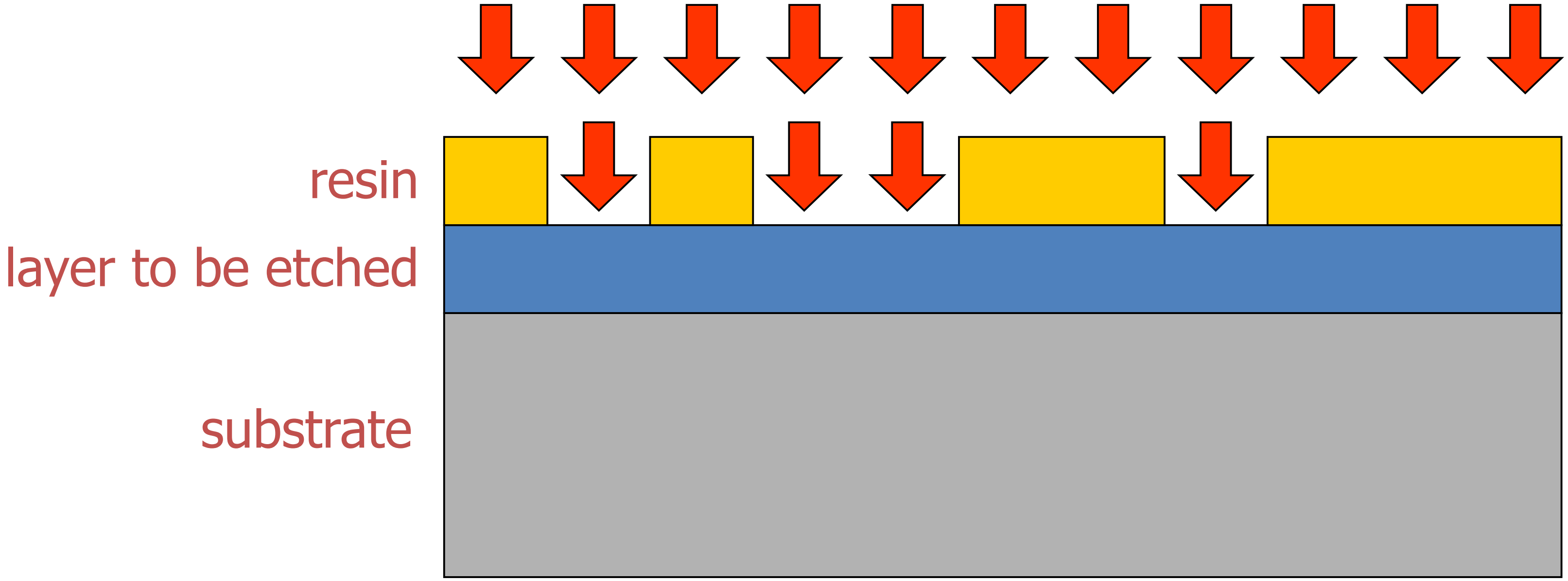
Photolithography

3) development: cleaning the exposed zones



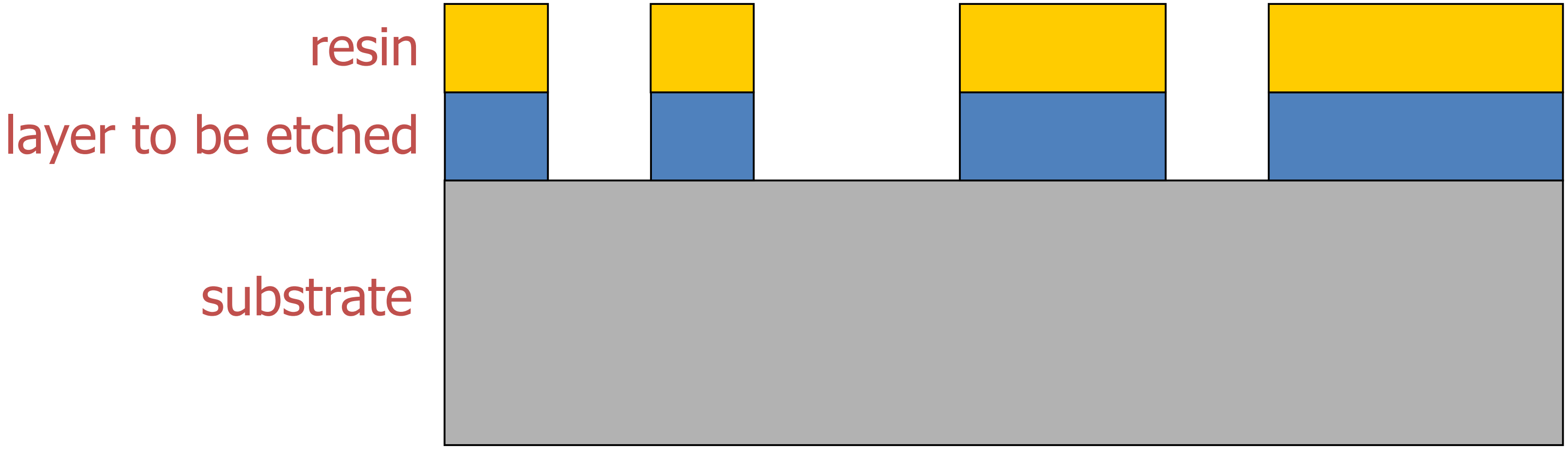
Photolithography

4) etching (ex: plasma)



Photolithography

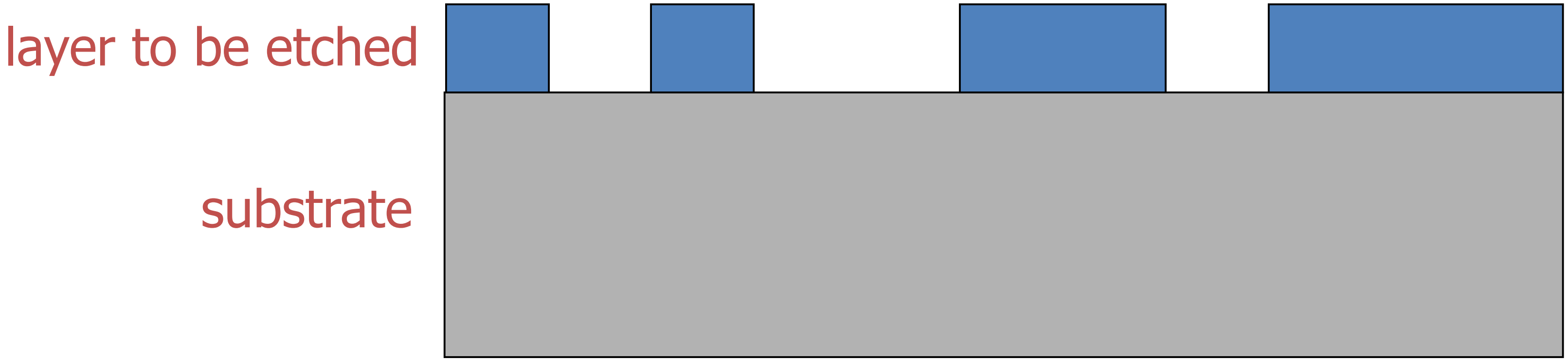
4) end of etching



Photolithography

5) after cleaning of the remaining resin

- pattern has been transfered onto the substrate



Photolitograpy

mask

- mask = original of the pattern to be transfered
- very costly (a few k€/mask)

- issue
  - diffraction limits the minimum size of the pattern
  - => smaller patterns require light of lower wavelength
- evolution
  - X-ray lithography
  - electron-beam lithography

Adding a new material

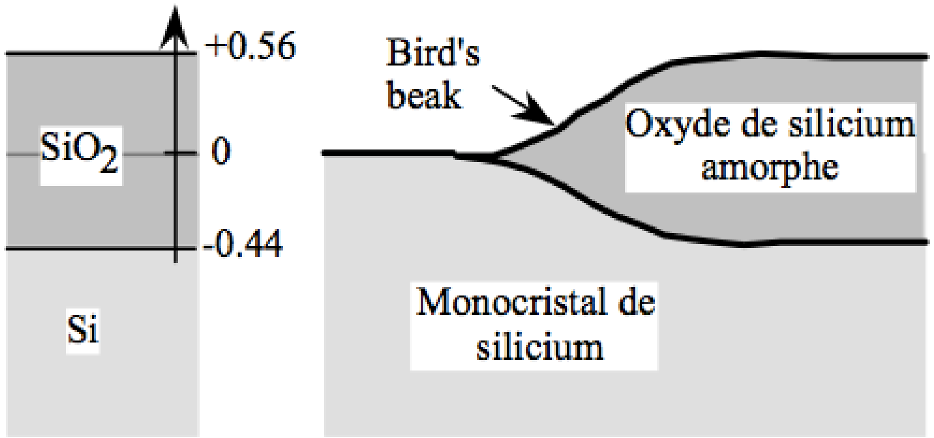
oxydation

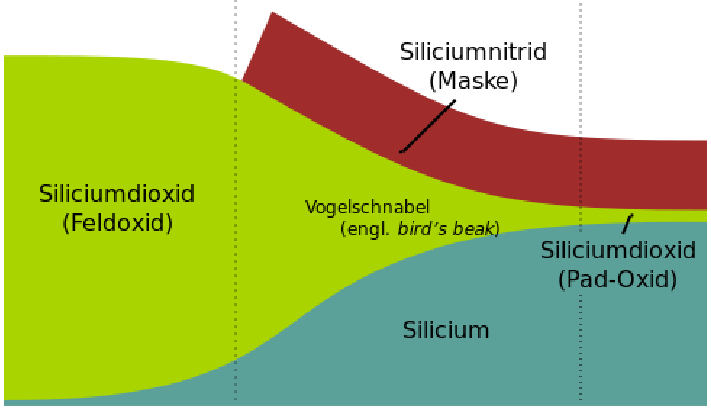
- Principle
  - growth of amorphous SiO_2 on Si wafer
    - chemically: very stable
    - electrically: excellent insulator
- Uses
  - passivation layer
  - field oxide (inert zone between active zones)
  - grid oxide (MOS transistors)
  - thin oxide (dielectric for capacitors)

Adding a new material

oxidation: "bird's beak" profile

- the oxide layer burries itself in the Si:





Adding a new material

Oxydation: technical details

- oxidation: oven at 1100° C
- dry oxidation
  - agent : O_2
  - 0,2µm SiO_2 / h
  - for grid oxide (very good quality) growth
- wet oxidation
  - agent : H_2O
  - 3µm SiO_2 / h
  - other oxides (more porosity)

Adding a new material

CVD: Chemical Vapor Deposition

- Principle:
  - laying down a non-metallic material: polysilicon, oxides, silicon nitride
  - chemical process to make an agent (initially in a gas) grow on the wafer

Adding a new material

Polysilicon deposition

- polycristalline Si deposition
  - SiH_4 carrying gas
  - 650° C
- uses
  - MOS grids + connected "wires"
  - second conductive layer

Adding a new material

PYROX et SILOX oxides deposition

- SiO_2 , P_2O_5 (PyroGlass), etc deposition
  - 400° C to 900° C
- uses
  - insulating layers
  - PyroGlass = final passivation layer
  - (don't mix up with the *oxidation* = SiO_2 *growth* on the wafer)

Adding a new material

Nitride deposition

- growth of Si_3N_4
  - 700° C to 900° C
- uses
  - obtain a thick oxide to insulate passive regions of the circuit from the substrate
  - passivation layer

Adding a new material

Epitaxy

- Principle
  - growth of an additional layer of Si extending the initial cristal structure (growth of the substrate)
  - layer of 3 to 10µm becoming the usable thickness to implant circuit elements
- advantage
  - doping profile impossible to obtain by other ways
- technical process
  - Si brought by gas (higher T° than CVD)

Adding a new material

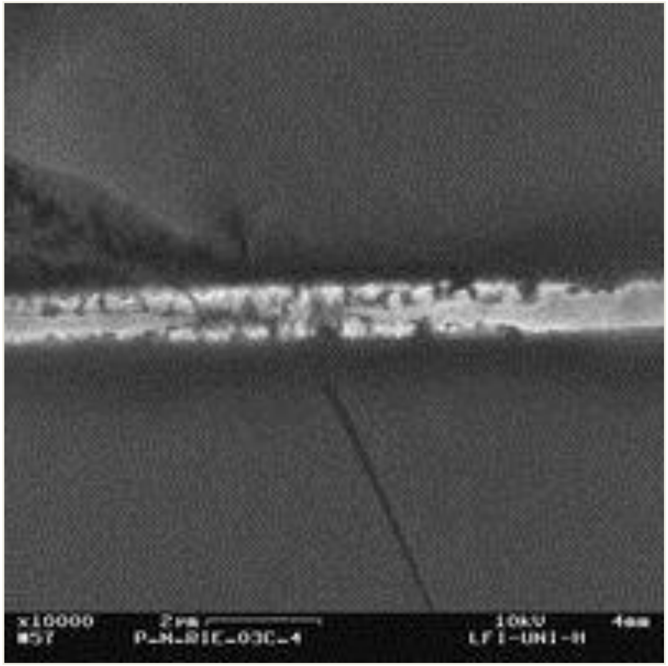
Metallization

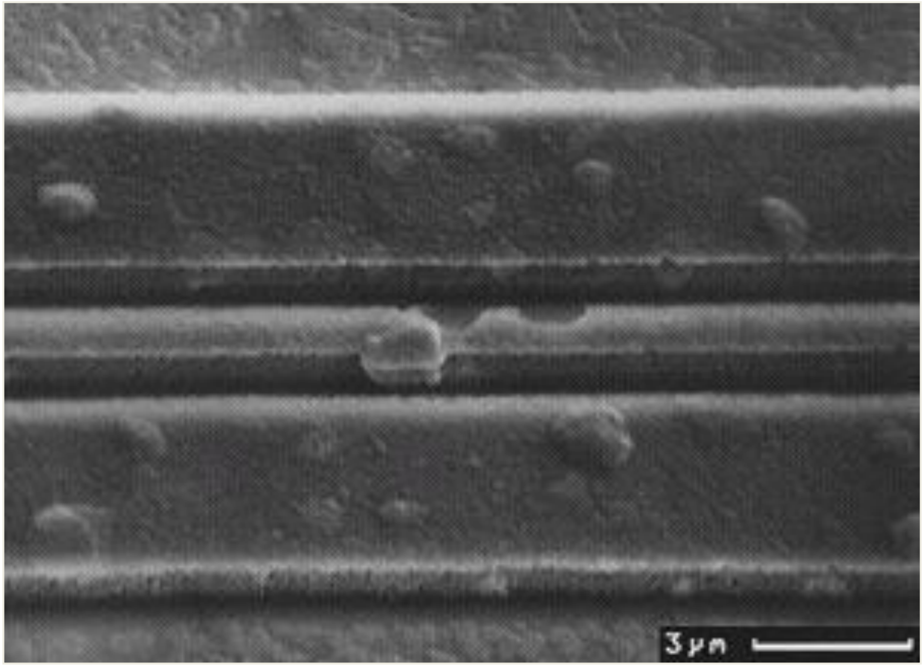
- principle
  - laying down metallic material (Al)
  - principle similar to CVD
- use
  - conductive connexions (lowest resistivity)
- issues
  - Al fusion T° = 650°C (low!)
  - Al subject to electromigration

Adding a new material

electromigration

- electromigration
  - destructive phenomenon (atoms pulled out) for high current densities inside wires (>1 mA/μm^2)
    - may lead to degradation or total rupture of connexion
    - considering miniaturization, these densities may occur





Adding a new material

interconnexions: alternatives to metals

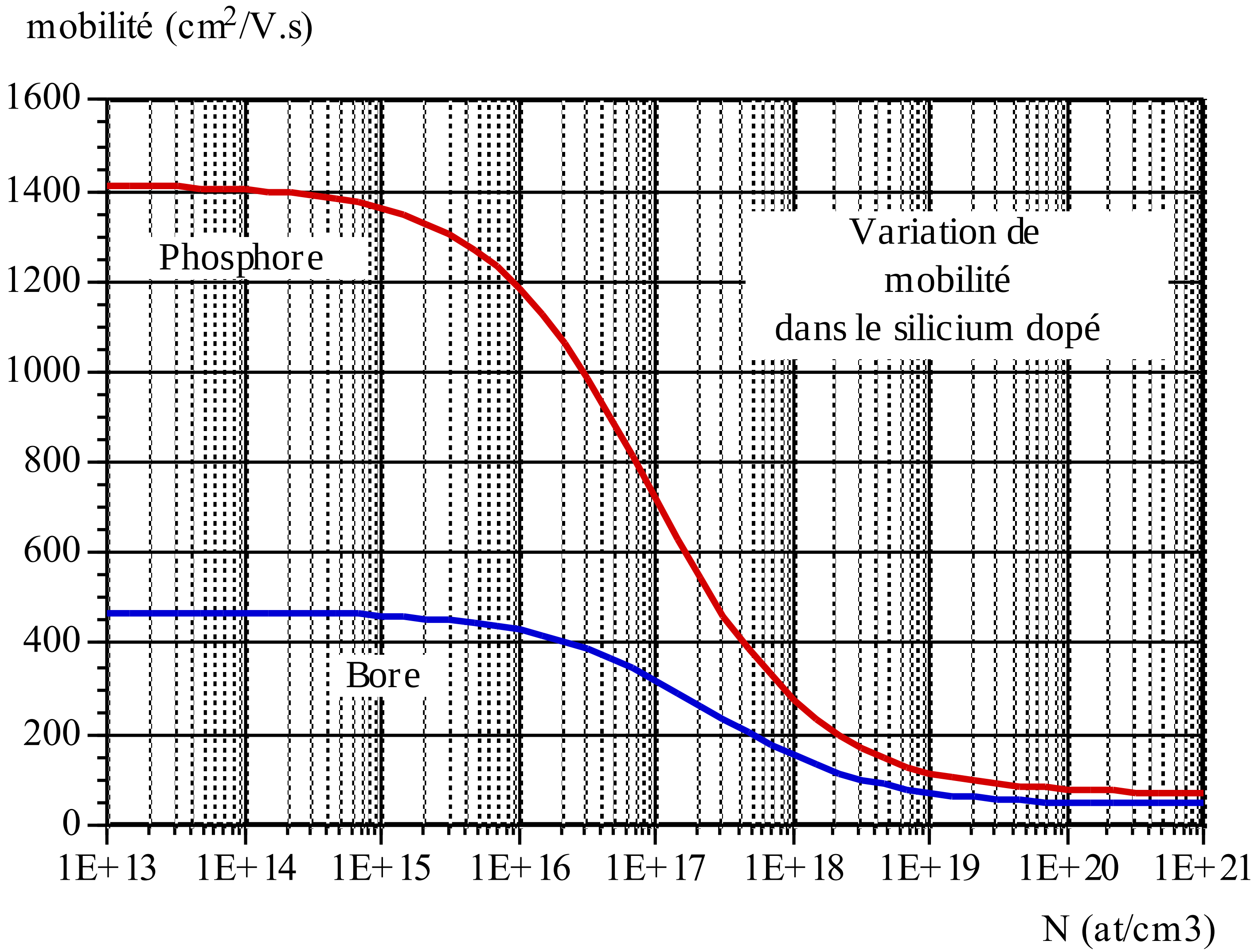
- polysilicon
- silicides
  - ceramics ($MoSi_2$, $TaSi_2$, $TiSi_2$, WSi_2, etc)
  - advantage: higher fusion T°
  - drawback: higher resistivity
- technologies with multiple metal layers

Doping

- principle
  - inserting extra atoms of different nature to locally modify the conductivity of Si
  - => N and P regions more or less doped
- doping atoms
  - atoms giving e^-: Sb, P, As
  - atoms receiving e^-: B, Al, Ga
  - 100% atoms are ionized @ ambiant T°
  - usual doping density: 10^{14} to 10^{21} at/cm^3
    - a low dopant concentration is enough to fix the overall Si conductivity

Doping

… and mobility



Doping

… and mobility

- MOS channel is lightly doped material
  - because gain is proportionnal to mobility
  - and high mobility obtained for low doping
- N-channel type MOS are preferred
  - because mobility obtained with N doping is higher than mobility obtained with P doping
- MOS drain and source are heavily doped for high conductivity (low resistance)

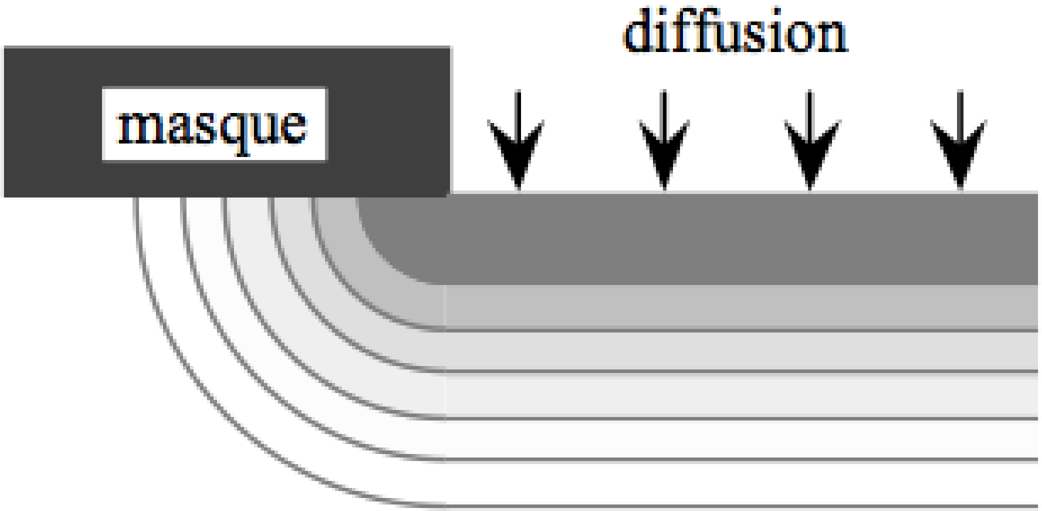
Doping

… by diffusion

- Reminder: diffusion
  - generic phenomenon: reorganisation of a group of mobile "particules" due to a spatial gradient of concentration $\frac{dn}{dx}$
- 2 steps:
  - predeposition (C_{surf} = constant)
    - carrier gas (dopants) constantly renewed
    - purpose: introduce a defined amount of carriers in the material
  - drive-in
    - neutral atmosphere
    - purpose: equalisation of concentrations near the surface

Doping by diffusion

Under-diffusion



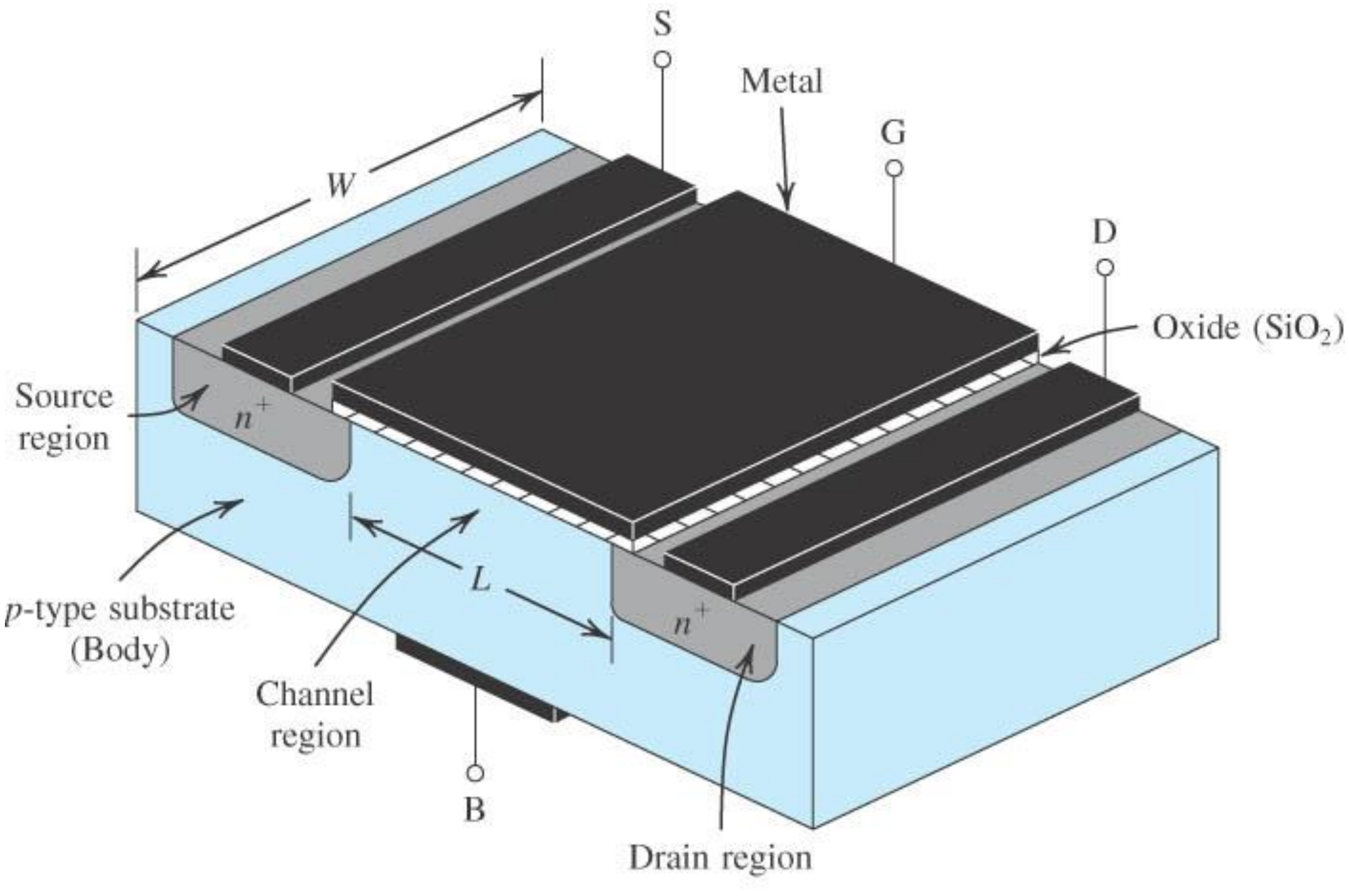
Doping

Doping via ionic implantation (>< diffusion)

- principle
  - Si is "bombed" by a beam of ions
- advantages (>< implantation via diffusion)
  - implantation depth controlled by beam energy
  - good precision on doping density
  - process at ambiant T°
  - good anisotropy
- drawback
  - need to repare the silicon from fractures caused by atomic collisions, by re-heating (annealing) the wafer

NMOS technology

Reminder



(a)

NMOS technology

You may implant…

- transistors: n-channel MOS
  - enhancement (Te)
  - depletion (Td)
- connexion wires/tracks
  - metal (M)
  - diffusion (D)
  - polysilicon (p)
- contact elements
  - metal/poly contact holes (C_p)
  - metal/diffusion contact holes (C_d)
- and nothing more!

NMOS technology

You may NOT implant…

- resistors
- capacitors
- diodes

- => nMOS technology not well suited for analog electronics

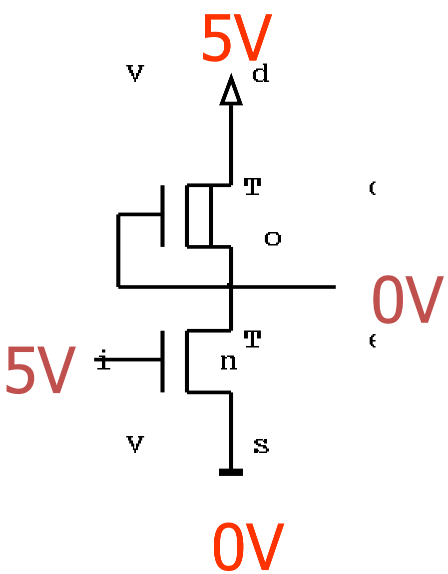
NMOS technology

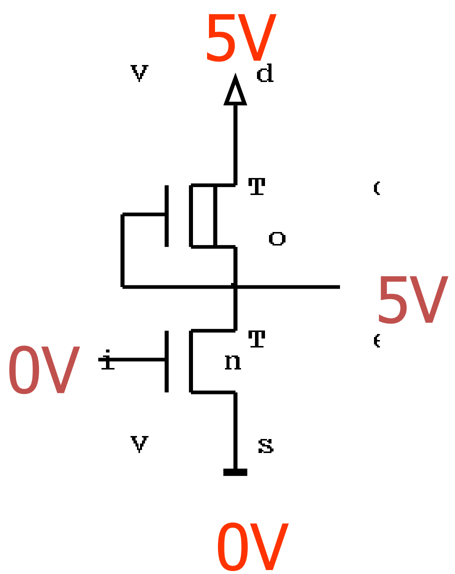
Reminder: Two types of NMOS transistors

- enhancement transistor (Te)
  - channel doped the same type as the substrate

  => spontaneously not conducting
- depletion transistor (Td)
  - channel doped the opposite type as the substrate

  ⇒ spontaneously conducting
- To build an inverter:

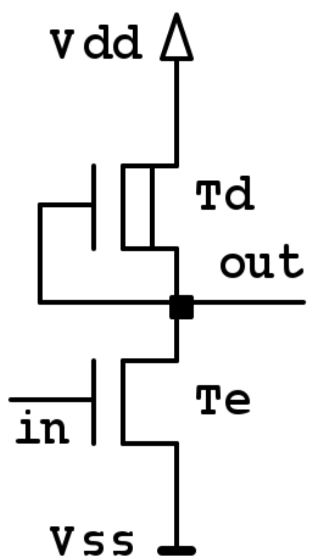




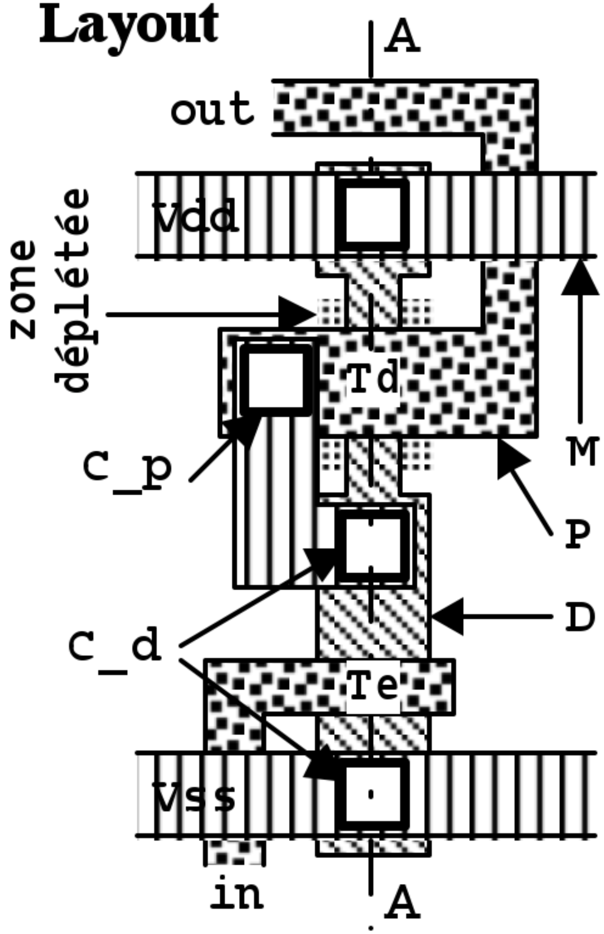
NMOS technology

At silicon level, the inverter becomes

Schéma



Layout



NMOS technology

To build such a structure, 6 masks are required…

- m#1: defines active zones >< field zones
- m#2: defines, in the active zones, where to invert the substrate type in order to later implant depletion transistors
- m#3: defines polysilicon layer pattern
- m#4: defines contact holes
- m#5: defines metal layer pattern
- m#6: defines contact pads (for connexions to the outside world)

NMOS technology

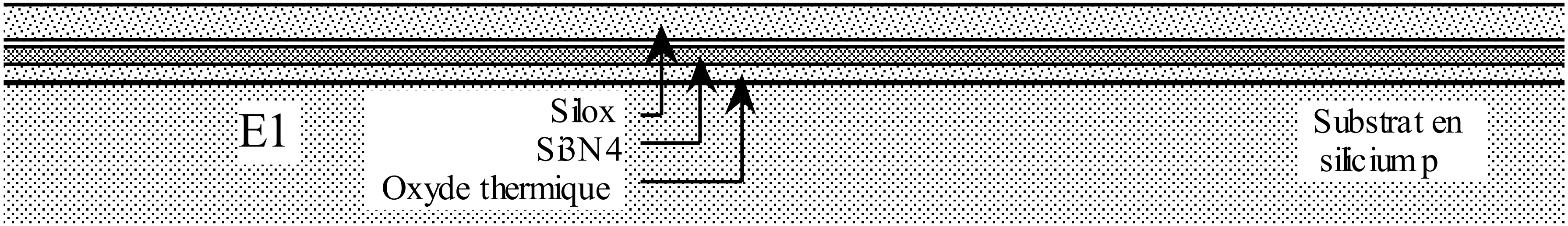
…and 18 steps of processing

- steps 1 to 6
  - implanting active zones and field zones
- steps 7 to 12
  - implanting transistors
- steps 13 to 18
  - adding metal connexions

NMOS technology

[E1] preparing the substrate

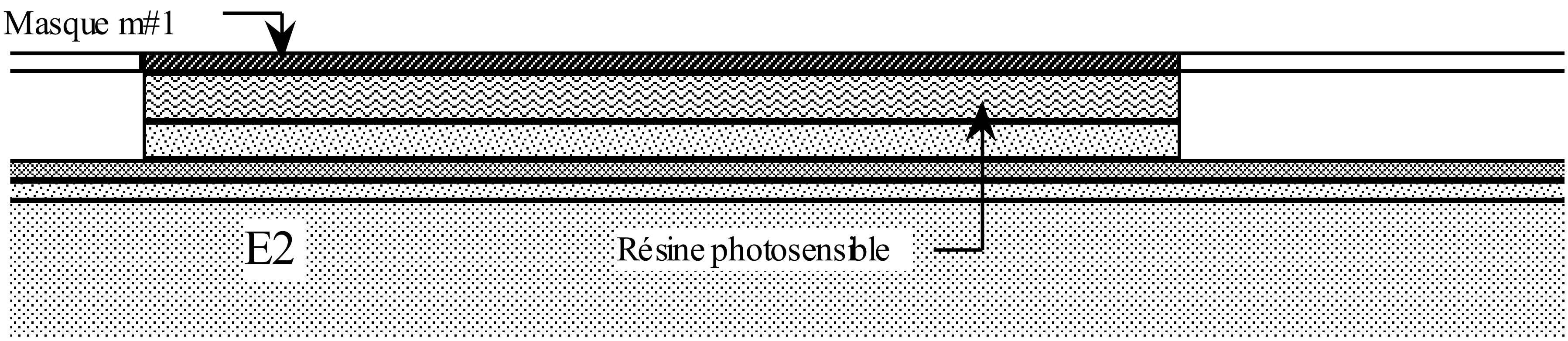
- growing 3 uniform layers



NMOS technology

[E2] defining active zones

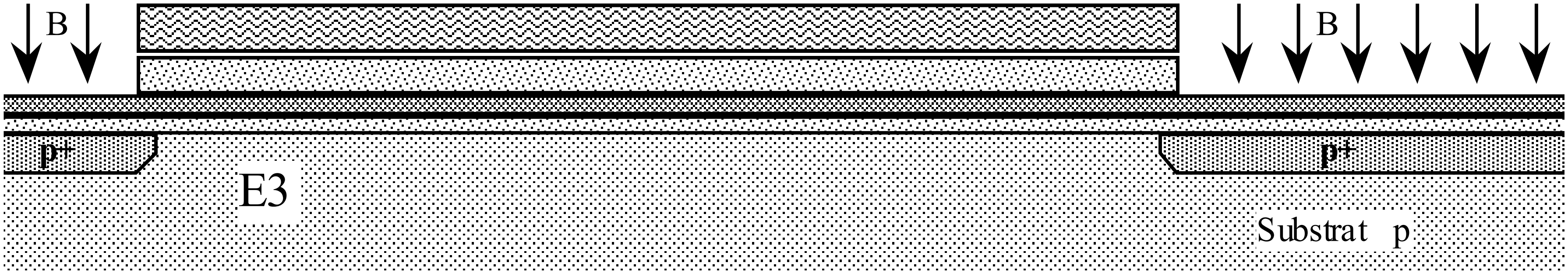
- photolithography (using m#1)
- fluorhydric acid (HF) etching



NMOS technology

[E3] doping the field zones

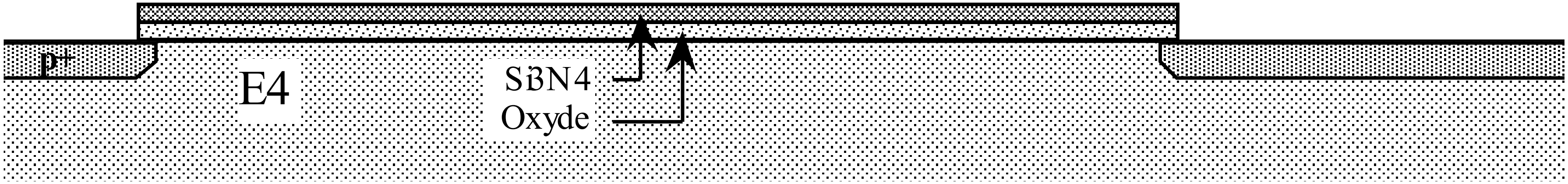
- p+ ionic implantation using boron (B)
  - inhibits possible inversion in field zones



NMOS technology

[E4] cleaning/removing…

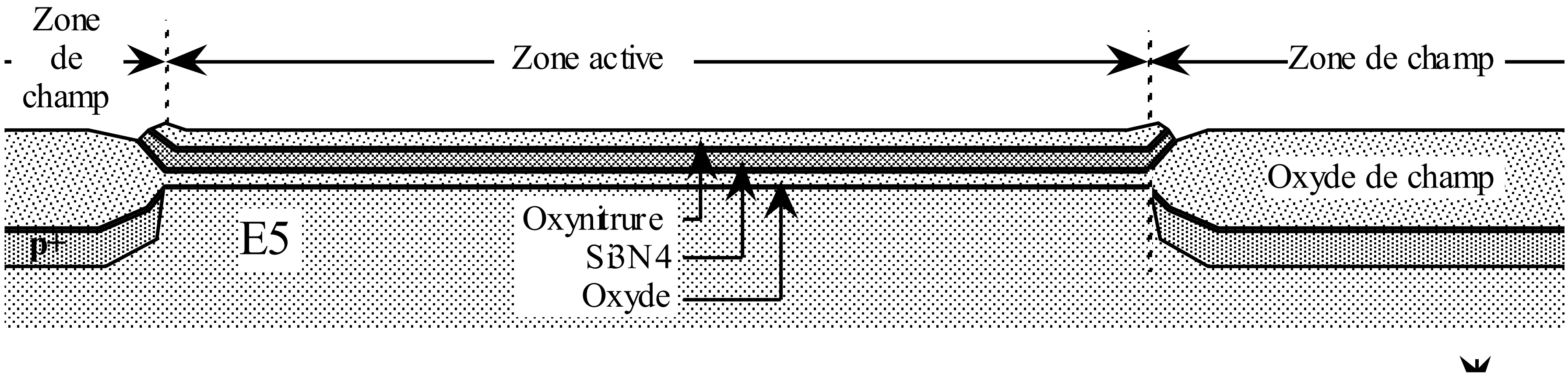
- … nitride in field zones (using H_3PO_4)
- … oxides (using HF)



NMOS technology

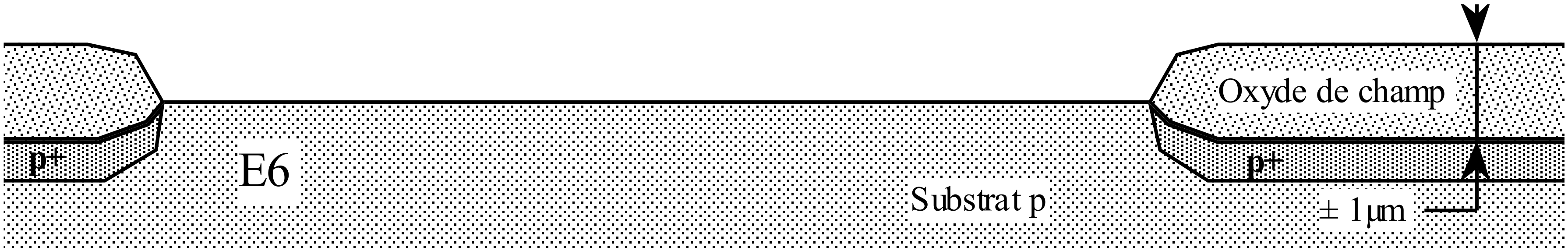
[E5] LOCOS process

- growing thick oxide (1µm) in field zones



NMOS technology

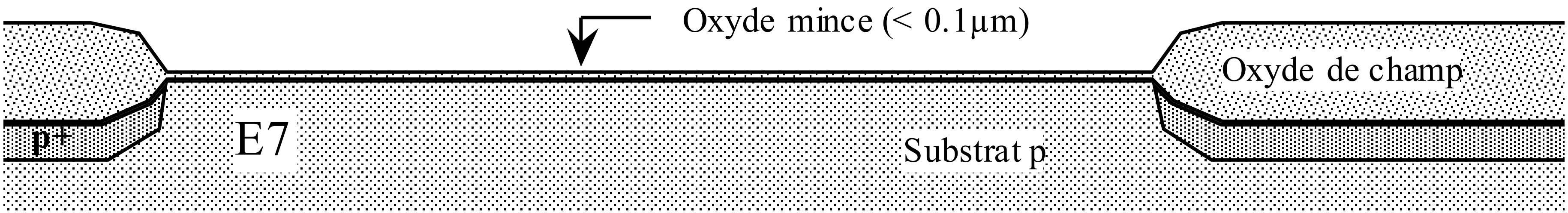
[E6] cleaning again…



NMOS technology

[E7] dry oxidation

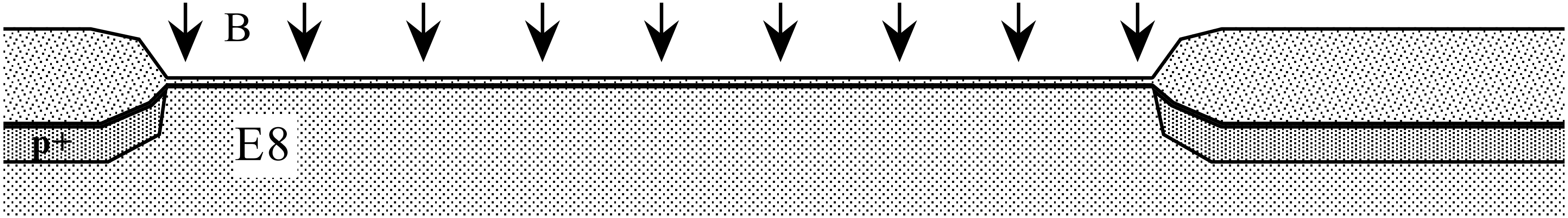
- growing grid oxide (thin oxide)



NMOS technology

[E8] raising threshold voltage (V_{T0})

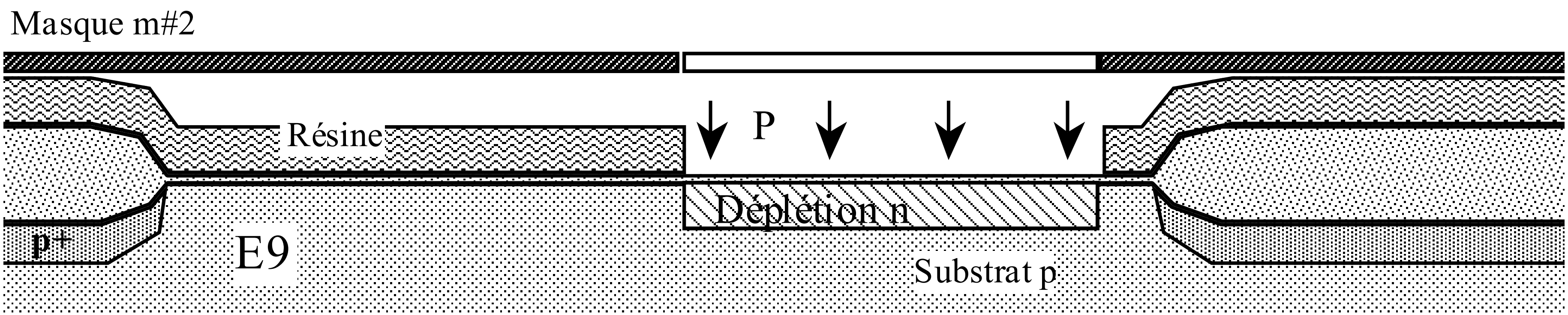
- from 0V to 1V
  - boron ionic implantation



NMOS technology

[E9] creating depletion zones

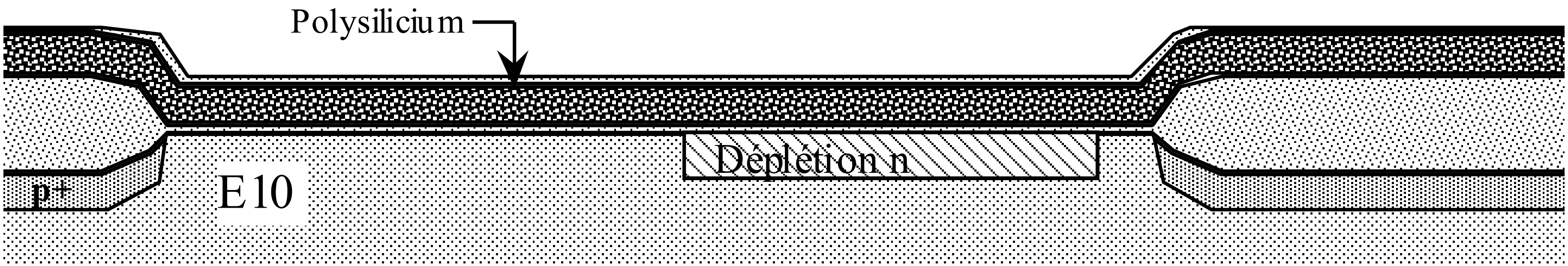
- photolithography (using m#2)
- phosphorus (P) ionic implantation
  - P diffuses in the substrate => depletion zones
  - intense doping to obtain high conductivity



NMOS technology

[E10] growing polysilicon

- will become the MOS grids

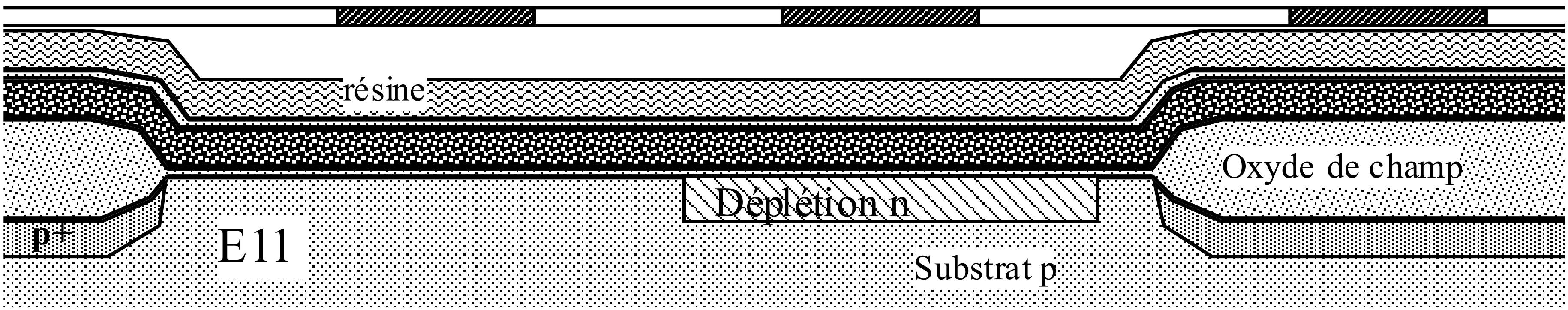


NMOS technology

[E11] poly etching

- photolithography (m#3)
- etches unprotected oxide and poly
- cleaning

Masque m#3

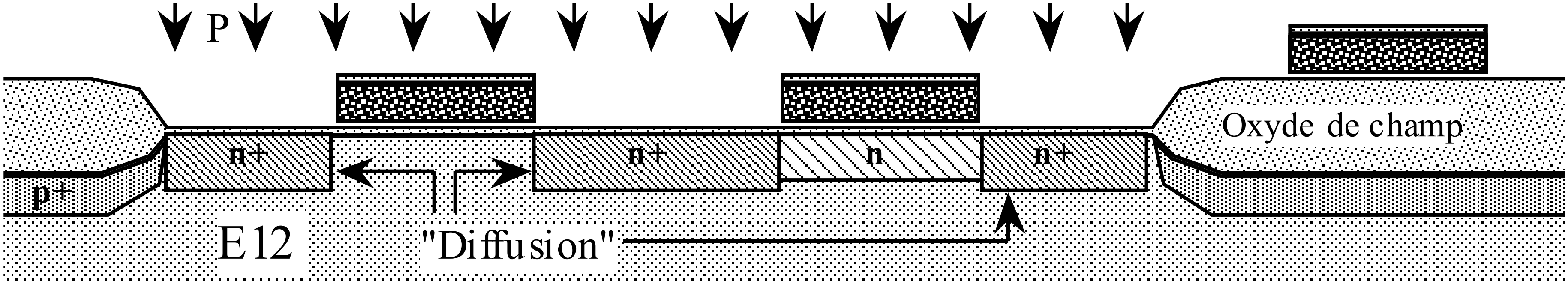


NMOS technology

[E12] implanting diffusion layer

- "diffusion" = deepest conducting layer of the IC

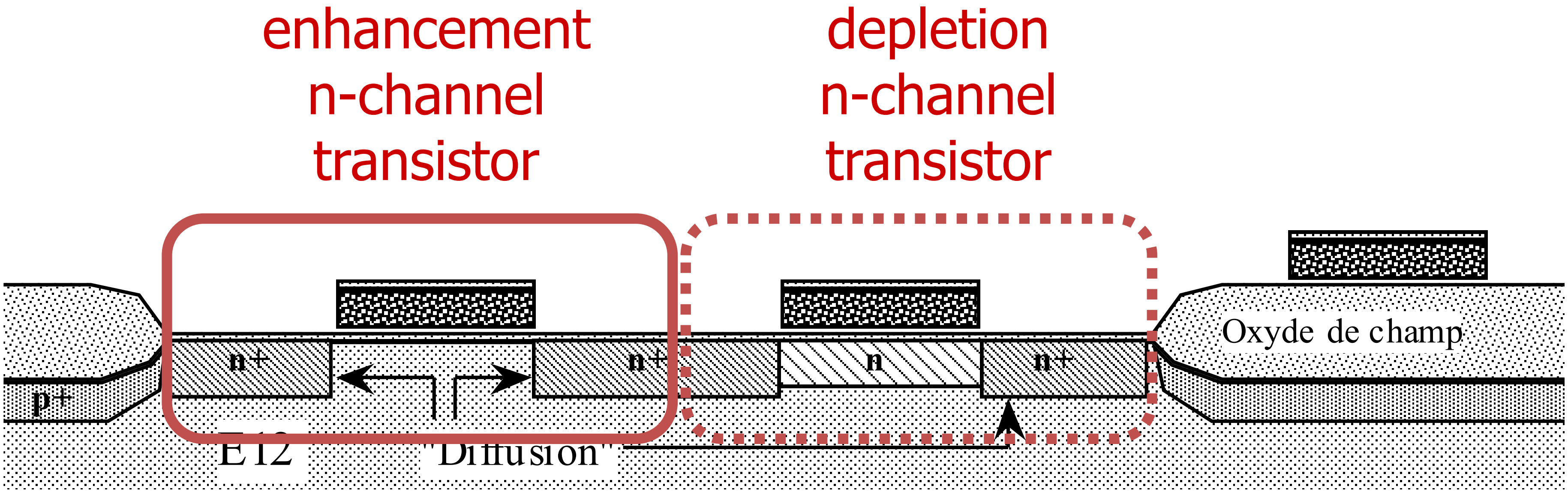
  = drains, sources and associated conducting wires
- using P ionic implantation (n+)



NMOS technology

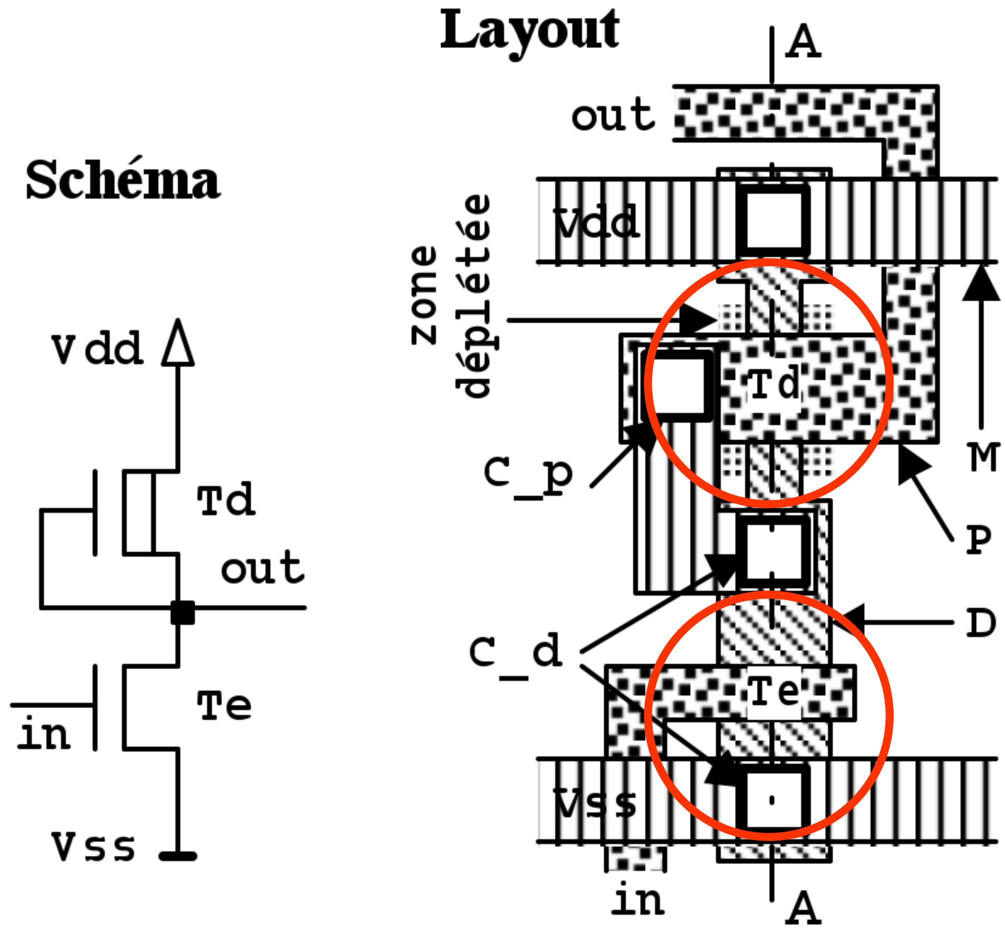
The inverter begins to appear

- Connexions still need to be made



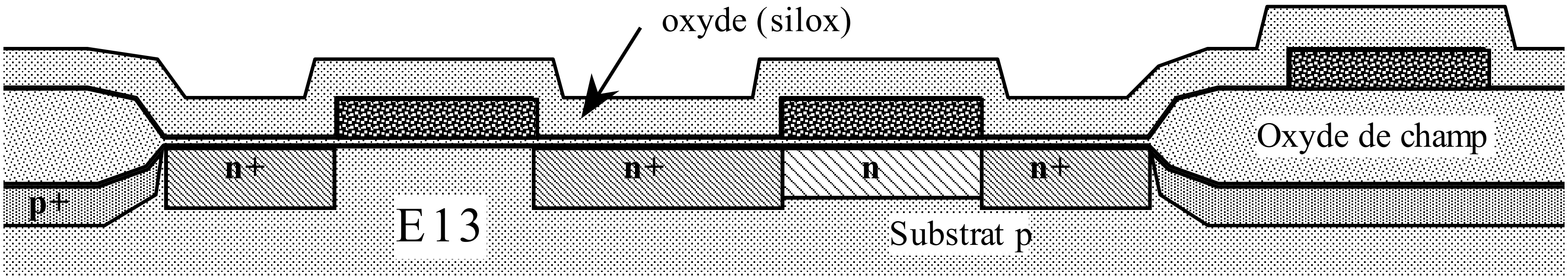
NMOS technology

- Transistors are at the crossing of poly (p) and diffusion (D)



NMOS technology

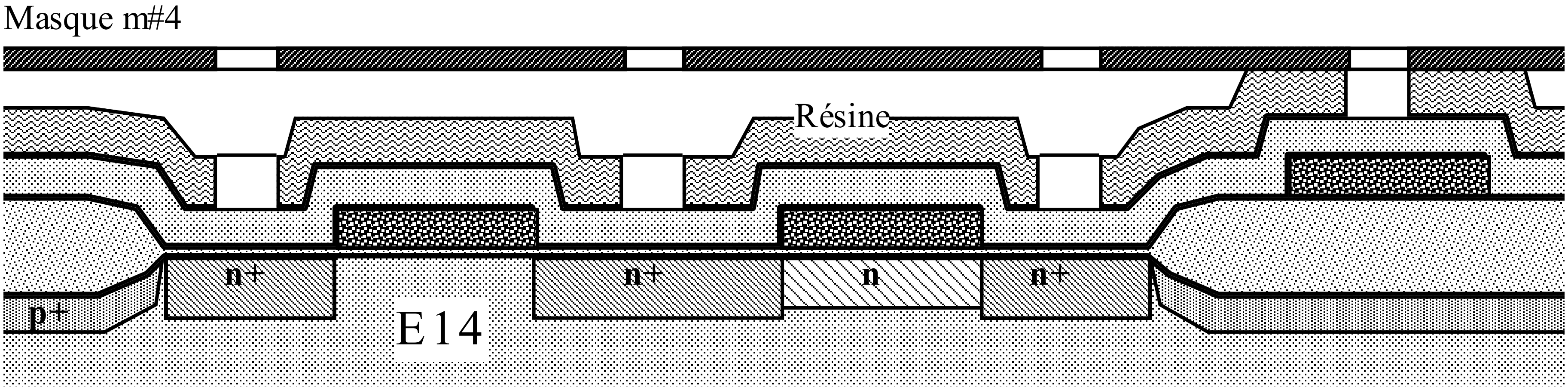
[E13] growing a silox layer



NMOS technology

[E14] defining contact holes

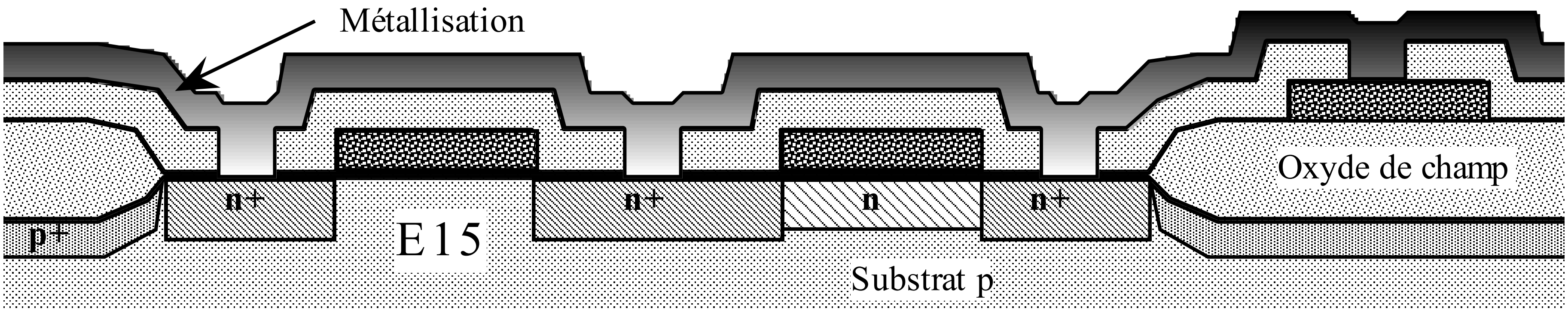
- photolithography (m#4)
- etching oxide
  - field zones: down to poly
  - active zones: down to substrate



NMOS technology

[E15] metal

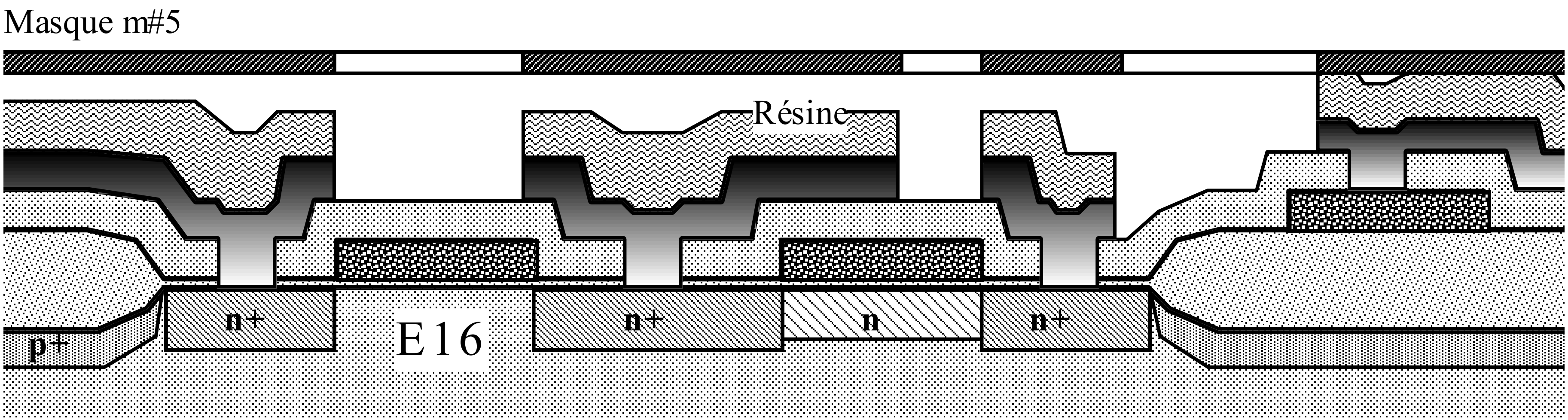
- uniform growth of Al layer



NMOS technology

[E16] defining metal connexions

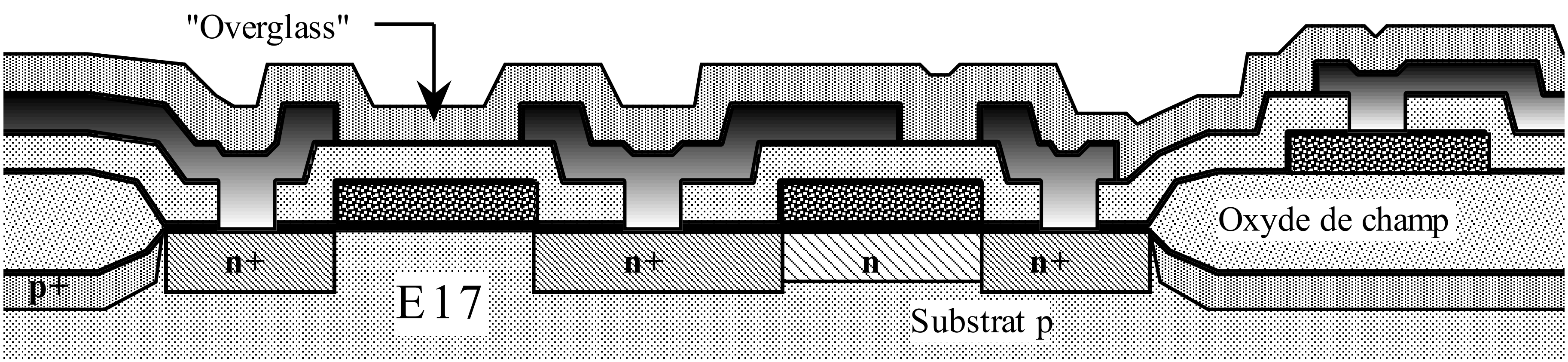
- photolithography (m#5)
- etching Al



NMOS technology

[E17] passivation

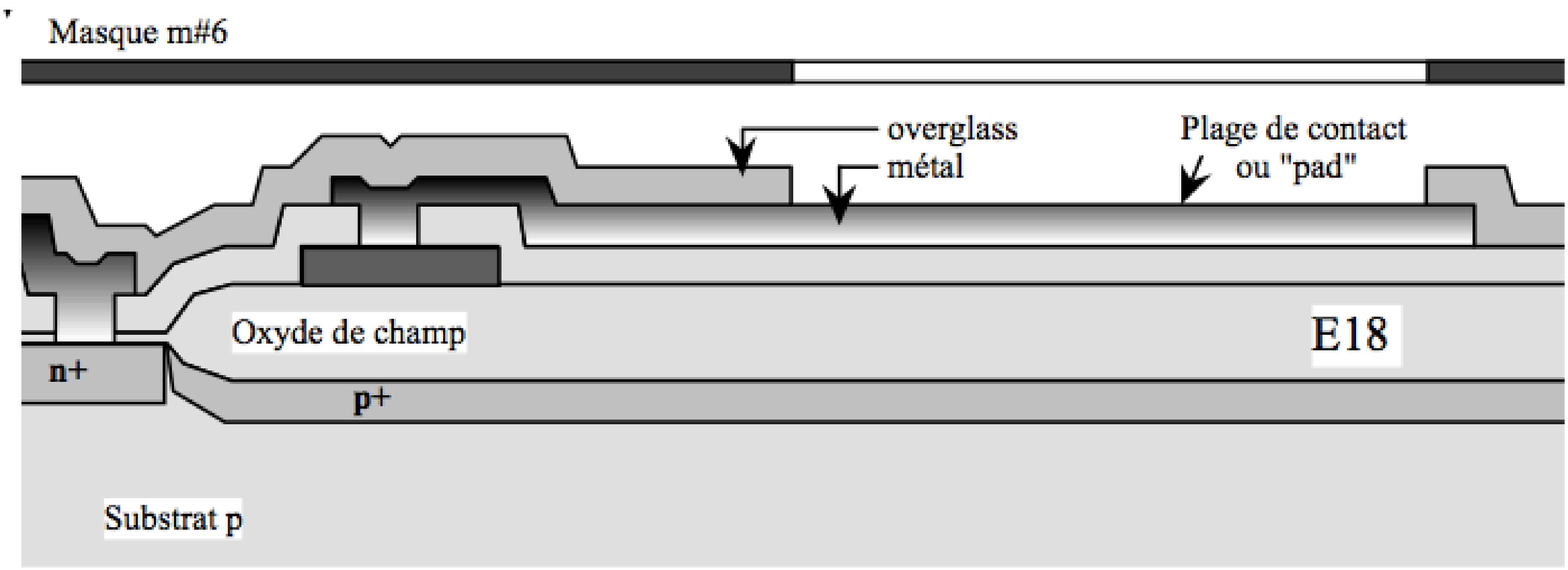
- uniform layer of pyroglass



NMOS technology

[E18] pad implantation

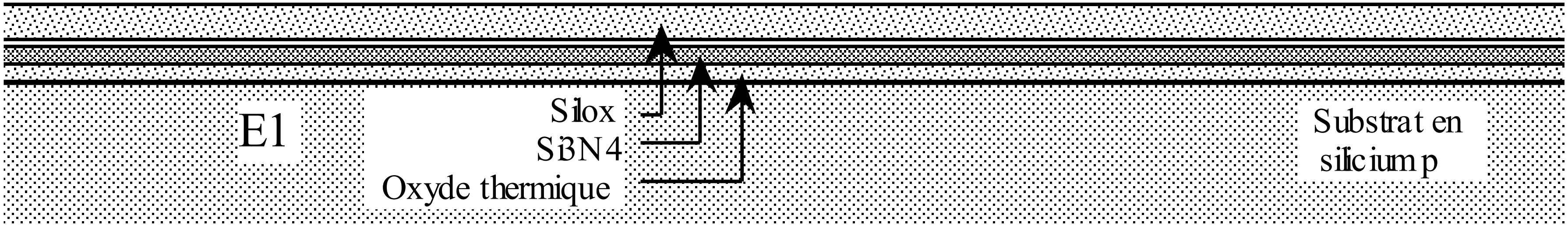
- photolithography (m#6) + etching
- pad = 100µm x 100µm



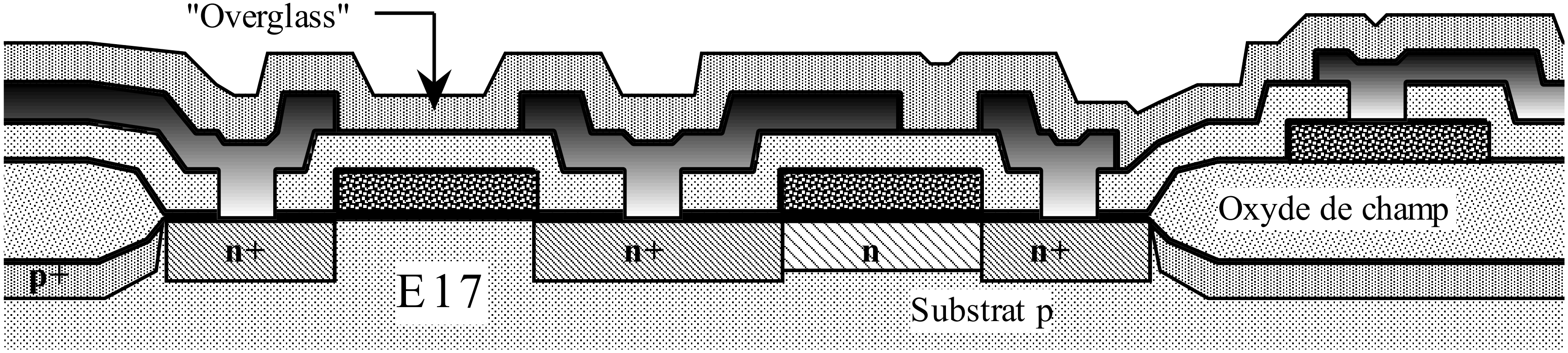
NMOS technology

18 steps

- **before…**

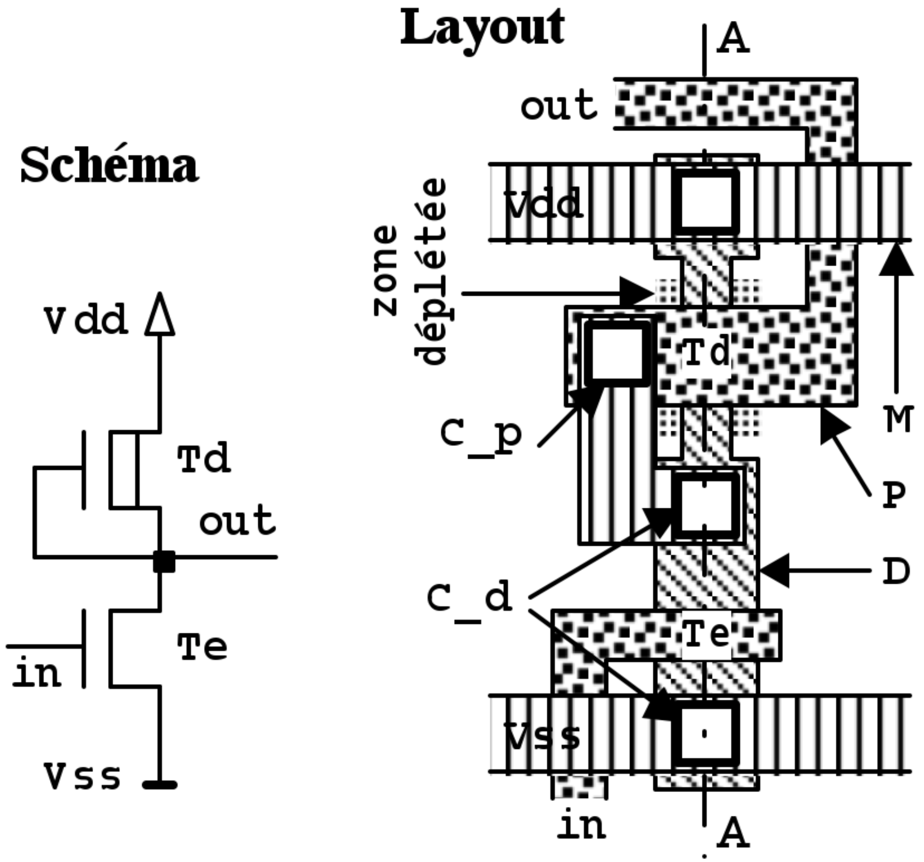


- **after…**



NMOS technology

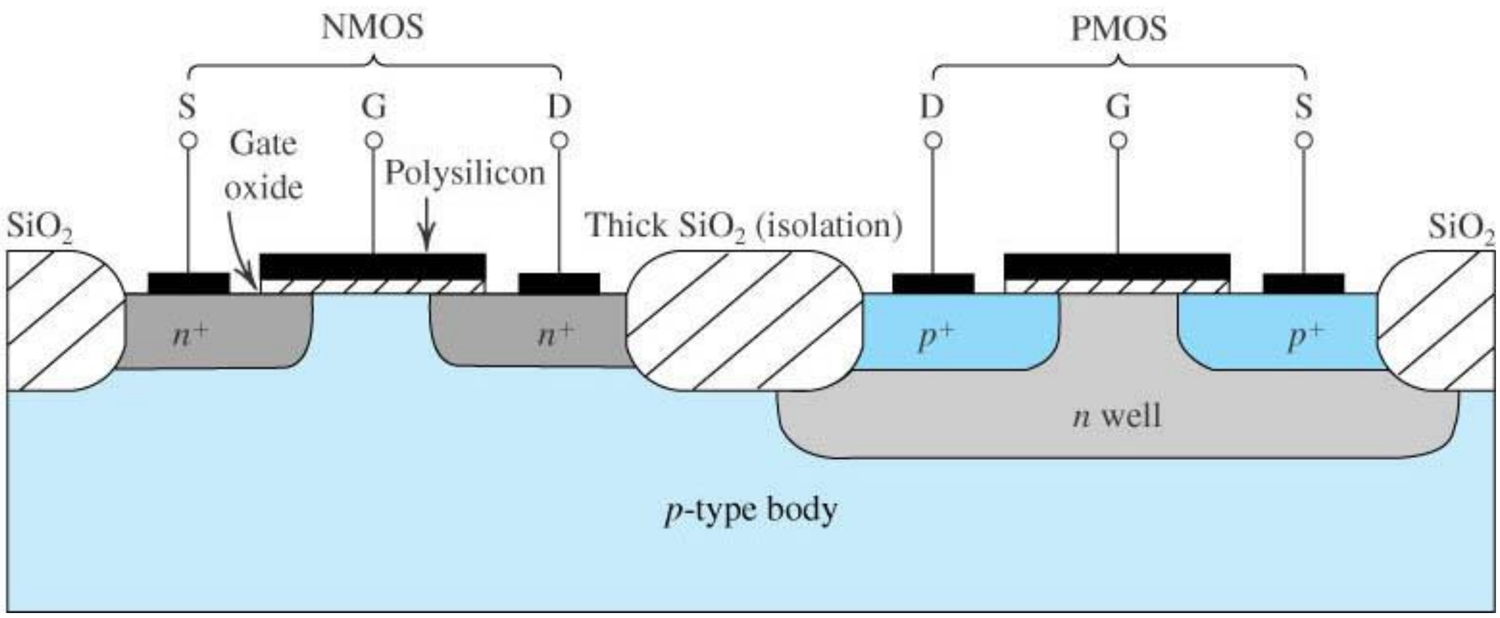
- The inverter is implanted and made of layers of materials



CMOS technology

Reminder

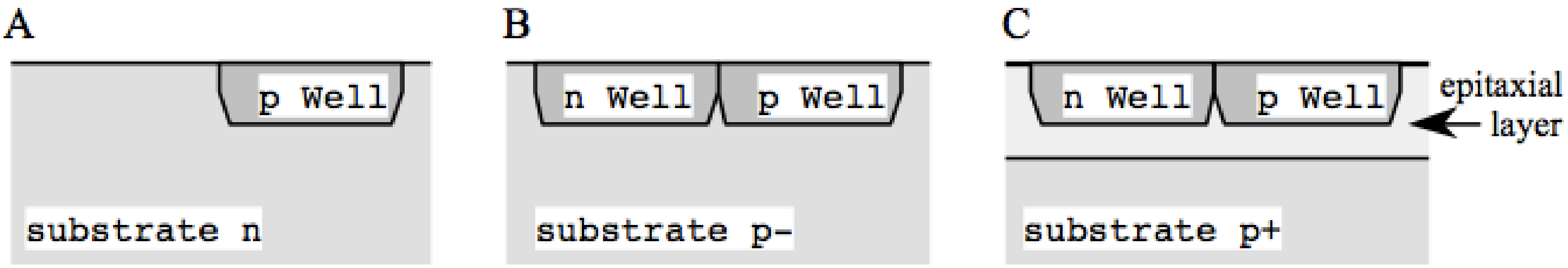
- Combination of NMOS and PMOS (e.g. logic inverter)



CMOS technology

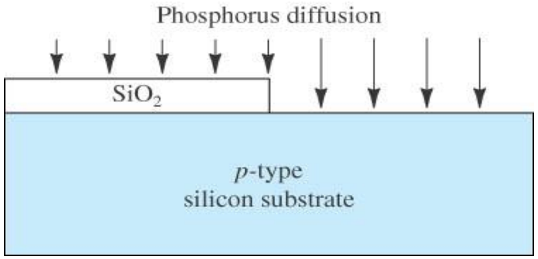
Implantable elements

- Presented technology
  - technology with p-Well and one layer of metal
- you may implant
  - n-channel and p-channel MOS transistors
  - p-type wells
  - connexions: metal, polysilicon, n-type diffusion and p-type diffusion
  - metal-diffusion and metal-polysilicon contacts
- well = locally inverted zone of the substrate

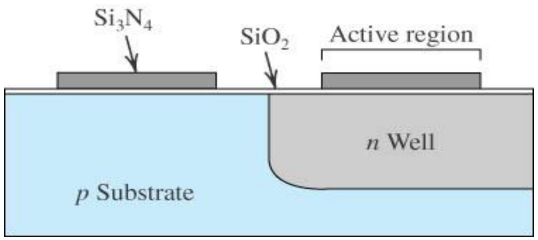


CMOS technology

- Mask #1: create the n-well

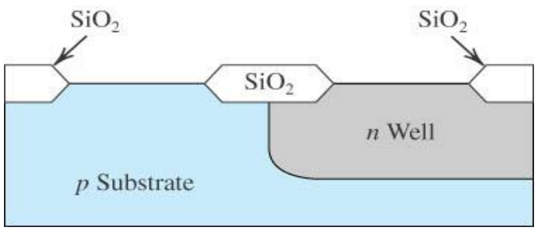


- Mask #2: define the active regions (areas w/o SiO2)

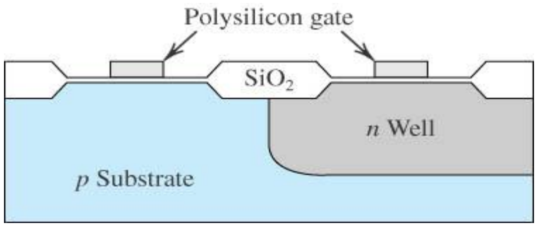


CMOS technology

- Local oxydation (make thick-field oxide appear to isolate transistors)

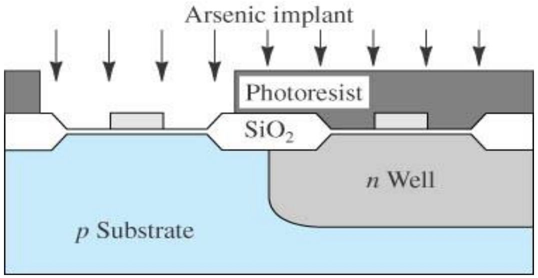


- Mask #3: Deposit polysilicon gate

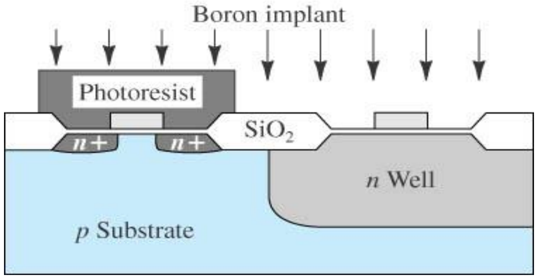


CMOS technology

- Mask #4: n+ diffusion

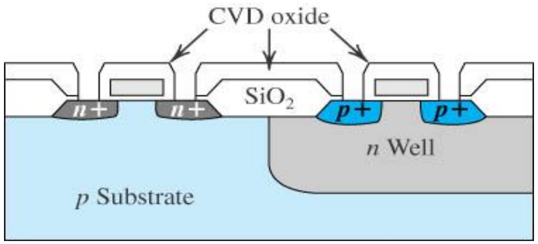


- Mask #5: p+ diffusion

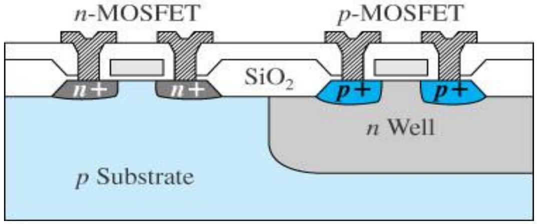


CMOS technology

- Mask #6: create contact holes

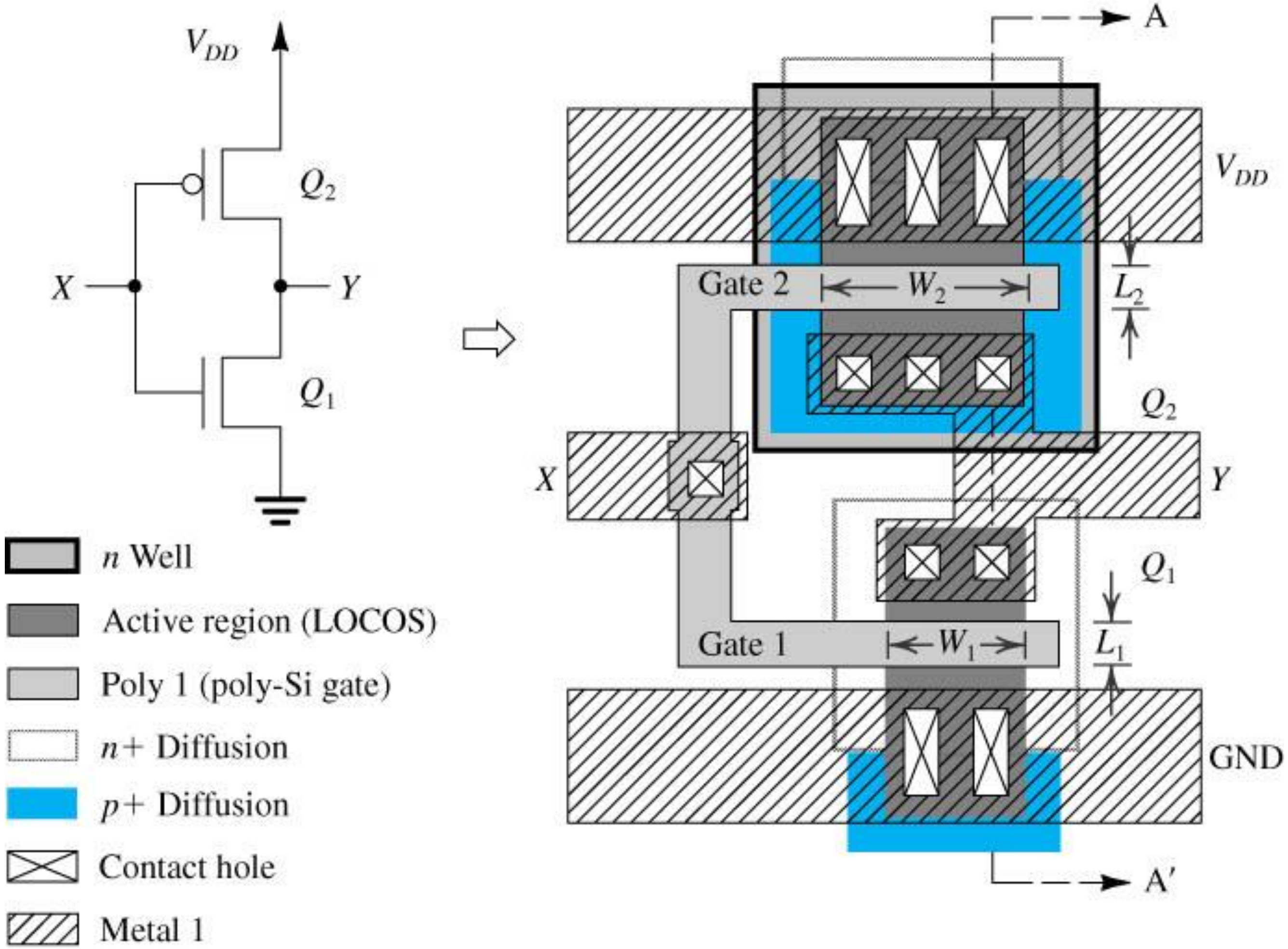


- Mask #7: deposit metallizations



CMOS technology

CMOS inverter layout



VLSI fabrication technology

Conclusions

- Many physico-chemical processes required
  - Good control of processes, especially for very small transistor sizes
  - Requires high purity (clean rooms) => high cost

- Many masks may be required
  - Increased risk due to mask misalignment
  - High cost of individual masks !