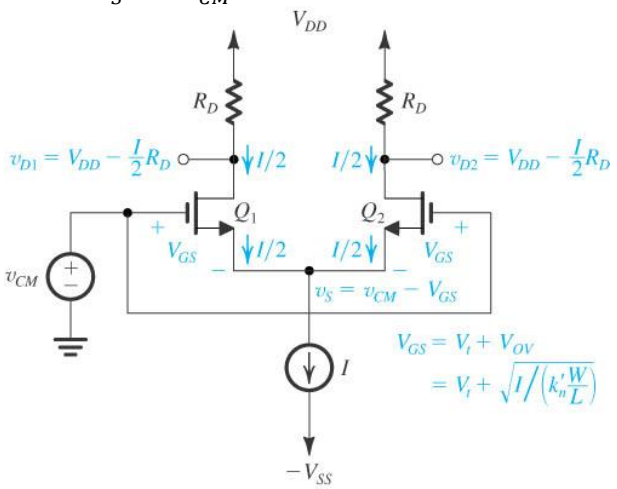
Chapter 5 : MOSFET differential amplifiers - exercices

MOS differential pair

Exercise 1 (7.1)

For an NMOS differential pair with a common-mode voltage v_{CM} applied, as shown in the figure, let $V_{DD} = V_{SS} = 2.5\ V$, $\frac{k'_n W}{L} = 3\ mA/V^2$, $V_t = 0.7\ V$, $I = 0.2\ mA$, $R_D = 5\ k\Omega$ and $\lambda = 0$.

a) Find V_{GS} for each transistor
b) For $v_{CM} = 0$, find $v_S, i_{D1}, i_{D2}, v_{D1}$ and v_{D2}
c) Repeat b) for $v_{CM} = 1$ V
d) What is the highest value of v_{CM} for which both transistors remain in saturation?
e) If the current source requires a minimum voltage of 0.3 V to operate properly, what is the lowest value allowed for v_S and v_{CM} ?



Exercise 2 (7.3)

For the differential amplifier from the previous exercise, let $v_{G2} = 0$ and $v_{G1} = v_{id}$. Find the value of v_{id} that corresponds to the following cases, and calculate (for each case) v_S, v_{D1}, v_{D2} and $v_{D2} - v_{D1}$.

a) $i_{D1} = i_{D2} = 0.1\ mA$
b) $i_{D1} = 0.15\ mA$ and $i_{D2} = 0.05\ mA$
c) $i_{D1} = 0.2\ mA$ and $i_{D2} = 0\ mA$ (Q2 in cutoff)

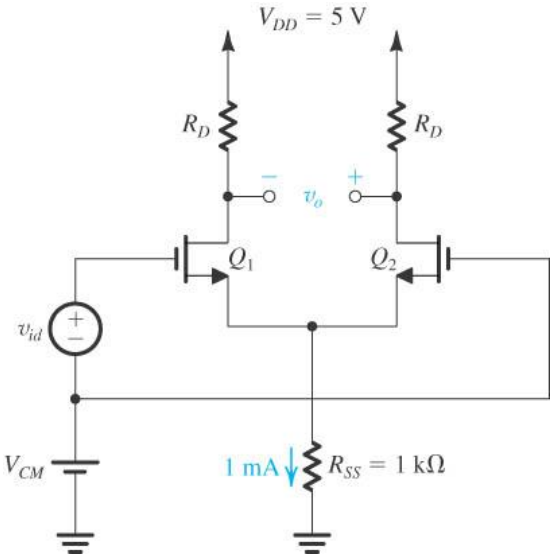
Exercise 3 (7.5)

Consider the differential amplifier from exercise 1 with G2 grounded and $v_{G1} = v_{id}$. Let v_{id} be adjusted to the value that causes $i_{D1} = 0.11\ mA$ and $i_{D2} = 0.09\ mA$. Find the corresponding values of v_{GS2}, v_S, v_{GS1} and v_{id}. What is the difference output voltage $v_{D2} - v_{D1}$? What is the voltage gain $(v_{D2} - v_{D1})/v_{id}$?

Exercise 4 (7.17)

The differential amplifier in the figure below utilizes a resistor R_{SS} to establish a 1-mA DC bias current. Note that this amplifier uses a single 5-V supply and thus needs a DC common-mode voltage V_{CM}. Transistors Q1 and Q2 have $\frac{k_n' W}{L} = 2.5\ mA/V^2$, $V_t = 0.7\ V$ and $\lambda = 0$.

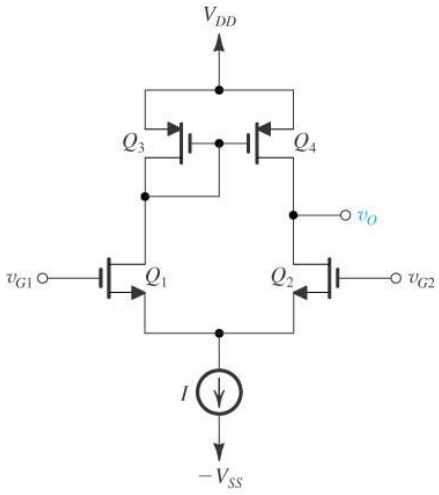
a) Find the required value of V_{CM}
b) Find the value of R_D that results in a differential vain v_o/v_{id} of 8.
c) Determine the DC voltage at the drains.
d) Determine the common-mode gain $\Delta V_{D1}/\Delta V_{CM}$ (hint: consider ΔV_{CM} small, and replace the circuit with its small-signal equivalent. Split the two branches of the circuit in two "half-branches, like in slide 19 of chapter 5.)



<u>Differential amplifier with active load</u>

Exercise 5 (7.62)

In an active-loaded differential amplifier of the form shown in the figure below, all transistors are characterized by $\frac{k_n' W}{L} = 3.2\ mA/V^2$ and $V_A = 20\ V$. Find the bias current I for which the gain $\frac{v_o}{v_{id}} = 80$



Exercise 6 (7.63)

For the MOS differential amplifier from previous exercise, all transistors have $\frac{k_n' W}{L} = 0.2\ mA/V^2$ and $V_A = 20\ V$. For $V_{DD} = 5\ V$, with the inputs near ground, and (a) $I = 100\ \mu A$ or (b) $I = 400\ \mu A$, calculate the g_m of Q1 and Q2, the output resistances of Q2 and Q4, the total output resistance and the voltage gain.

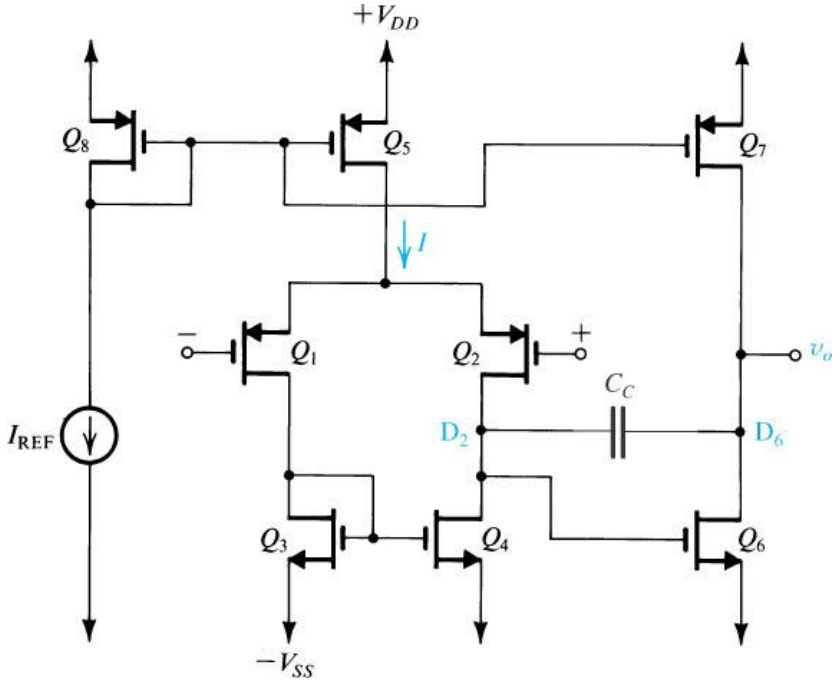
Multistage amplifiers

Exercise 7 (7.90)

Consider the circuit shown in the figure below, with the transistor geometries shown in the table. Let $I_{REF} = 225\ \mu A, |V_t| = 0.75\ V$ for all devices, $\mu_n C_{ox} = 180\ \mu A/V^2$, $\mu_p C_{ox} = 60\ \mu A/V^2$, $|V_A| = 9\ V$ for all devices, $V_{DD} = V_{SS} = 1.5\ V$.

a) Determine the width W of Q6 that will ensure that the op amp will not have a systematic offset voltage. To do this, connect both inputs to the ground, and evaluate the width W of Q6 such that the current consumed by Q6 is identical to the current delivered by Q7 (note that in this case, V_o is equal to zero). Use the fact that the differential amplifier is perfectly symmetric, such that $V_{D4} = V_{D3}$.
b) Using the width W of Q6 calculated in a), for all devices, evaluate I_D, V_{GS}, g_m, r_o. (put results in table)
c) Find the gains A_1 and A_2 of the first stage and second stage, respectively, and the total open-loop voltage gain.

Transistor	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
W/L	30/0.5	30/0.5	10/0.5	10/0.5	60/0.5	W/0.5	60/0.5	60/0.5


+V_DD
Q8
Q5
Q7
I
−
Q1
Q2
+
v_o
C_C
I_REF
D2
D6
Q3
Q4
Q6
−V_SS