Chapter 5

MOSFET differential amplifier

Outline

- Introduction
- Ideal MOS differential pair
  - Common-mode voltage
  - Large-signal operation
  - Small-signal operation
- Nonidealities
  - Common-mode rejection ratio
  - Input offset voltage
- Differential amplifier with active load
- Frequency response of differential amplifier
- Multistage amplifiers

Why a differential amplifier ?

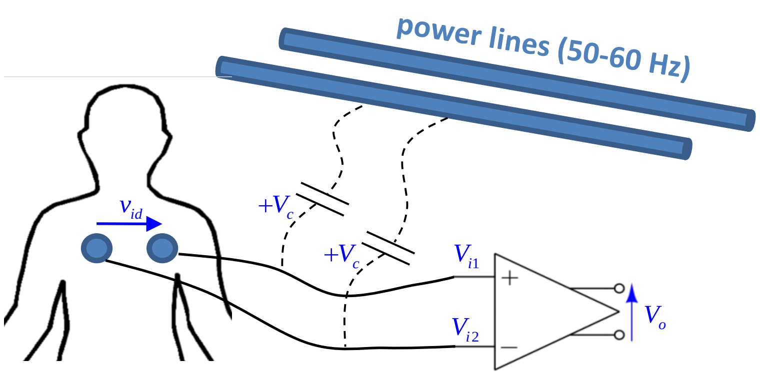
… *differential* voltage – polluted by common mode

- Many sensors provide a differential voltage

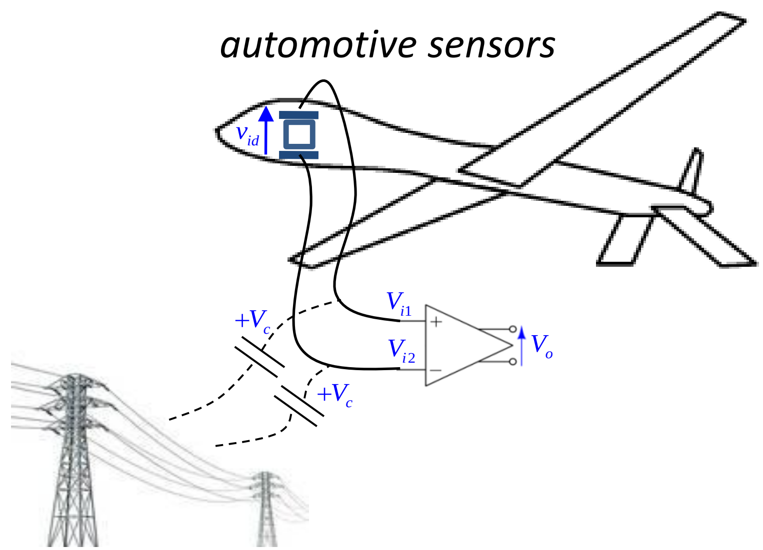
  $\Rightarrow$ When transmitting this differential voltage over cables, they become susceptible to common-mode voltage (power lines, RF interference, magnetic fields, …)

  $\Rightarrow$ Common-mode voltage also appears if ground of sensor is different from ground of circuit

  $\Rightarrow$ Differential voltage can be small w.r.t. common-mode voltage



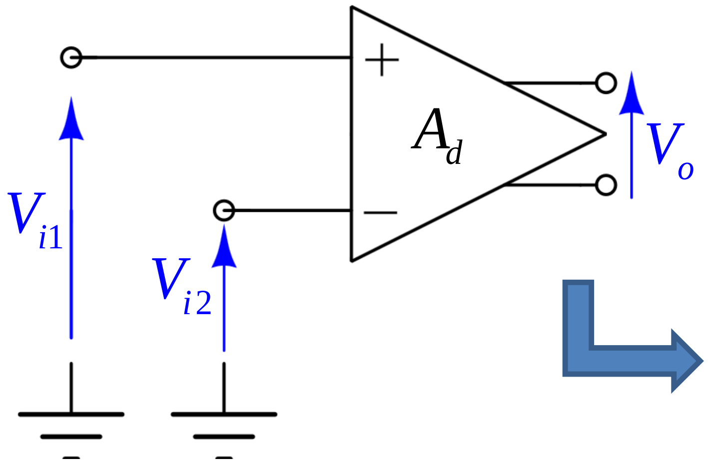
ECG



automotive sensors

Ideal differential amplifier

only amplifies the *difference* between input voltages



$$\begin{cases} V_{i1} = V_c + \dfrac{v_{id}}{2} \\ V_{i2} = V_c - \dfrac{v_{id}}{2} \end{cases} \Leftrightarrow \begin{cases} V_c = \dfrac{V_{i1} + V_{i2}}{2} \\ v_{id} = V_{i1} - V_{i2} \end{cases}$$

$$\begin{aligned} V_o &= A_c \cdot \left(\frac{V_{i1} + V_{i2}}{2} \right) + A_d \cdot (V_{i1} - V_{i2}) \\ &= A_c V_c + A_d v_{id} \end{aligned}$$

- Ideal differential amplifier
  - $\Rightarrow$ High differential gain Ad
  - $\Rightarrow$ Small common gain Ac
  - $\Rightarrow$ High input resistance

$$\boxed{V_o = A_d \cdot (V_{i1} - V_{i2})}$$

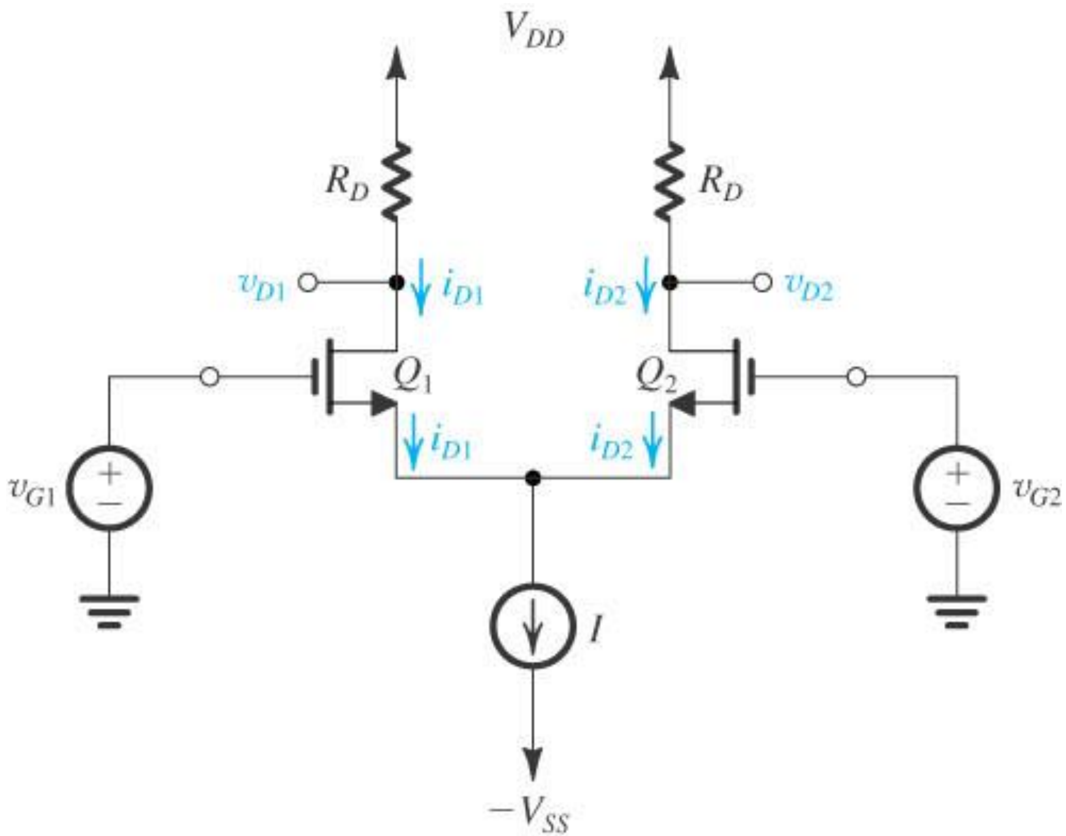
- How to build this in MOSFET technology ?

Ideal MOS differential pair

2 matched transistors, biased by current source

- 2 inputs are the two gates of the transistors

  $\Rightarrow$ High input impedance !!!



Assumptions:
- Transistors identical
- Drain resistors identical
- Perfect current source

Common mode and differential mode:

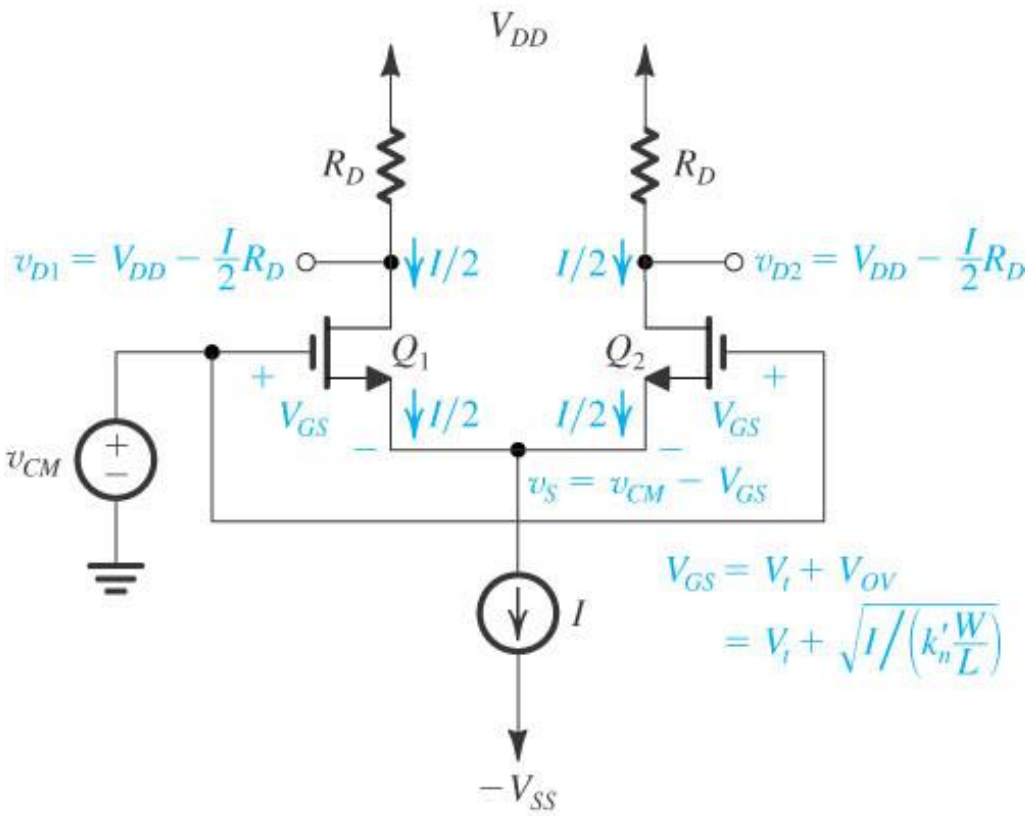
$$\begin{cases} v_{CM} = \dfrac{v_{G1} + v_{G2}}{2} \\ v_{id} = v_{G1} - v_{G2} \end{cases}$$

$$\Leftrightarrow \begin{cases} v_{G1} = v_{CM} + \dfrac{v_{id}}{2} \\ v_{G2} = v_{CM} - \dfrac{v_{id}}{2} \end{cases}$$

Ideal MOS differential pair

Common-mode input voltage

- Identical voltage at both inputs



Symmetry arguments:

$$i_{D1} = i_{D2} = I/2$$

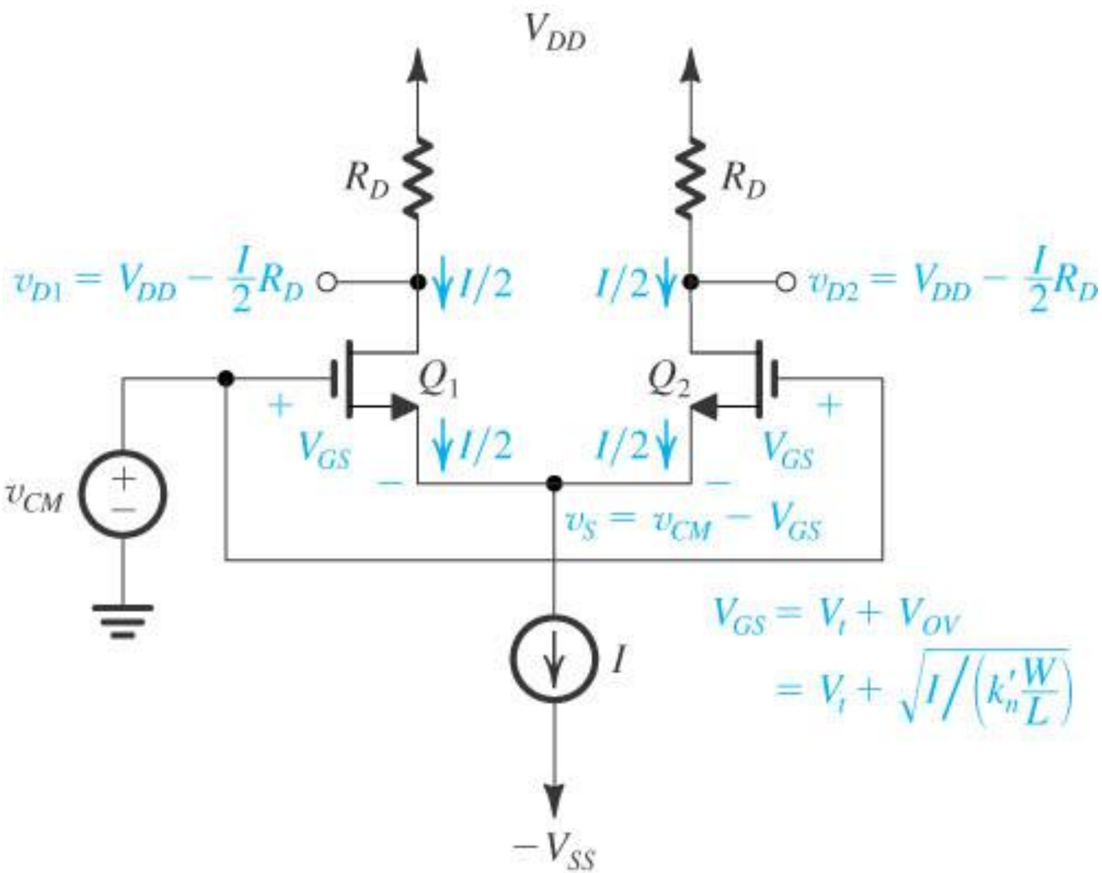
$$\Rightarrow v_{D1} = V_{DD} - R_D I/2 = v_{D2}$$

$$\Rightarrow v_o = v_{D2} - v_{D1} = 0$$

$\Rightarrow$ Common gain is zero

Ideal MOS differential pair

Max. and min. common-mode input voltage



Q_1 and Q_2 in saturation:

$$v_{DS} > \left(v_{GS} - V_t\right)$$

$$\Rightarrow V_{DD} - R_D i_D - v_S > v_{CM} - v_S - V_t$$

$$\Rightarrow \boxed{v_{CM} < V_{DD} - \frac{R_D I}{2} + V_t}$$

Current source must operate properly:

$\Rightarrow$ Minimum voltage V_{CS} over current source

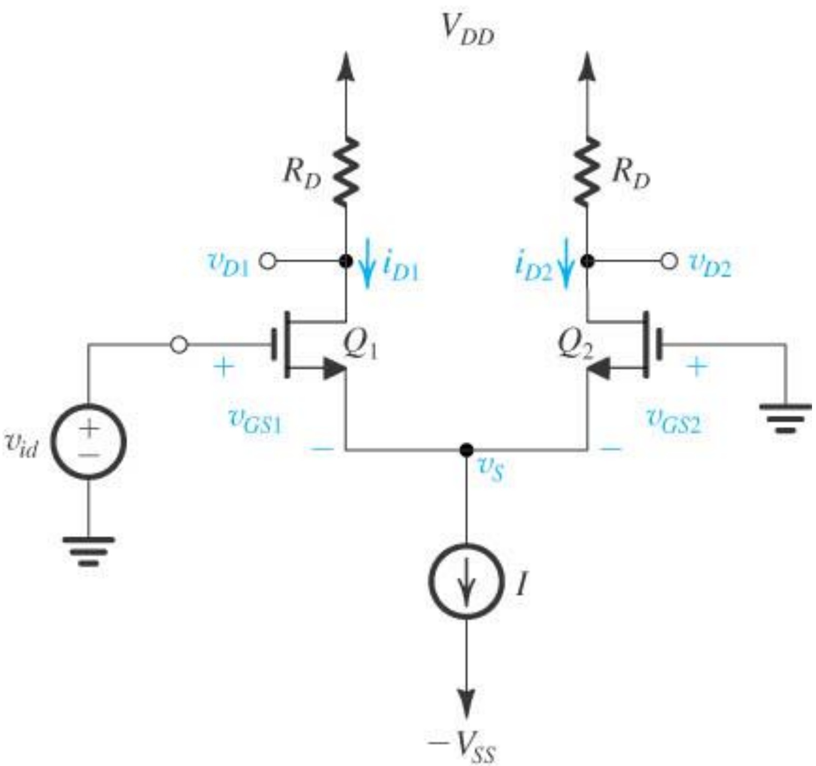
$$v_S - \left(-V_{SS}\right) > V_{CS}$$

$$\Rightarrow v_{CM} - V_{GS} + V_{SS} > V_{CS}$$

$$\Rightarrow \boxed{v_{CM} > -V_{SS} + V_{CS} + V_{GS}}$$

Ideal MOS differential pair

Differential input voltage: large-signal behavior



$$\begin{cases} v_{id} = v_{GS1} + v_S \\ 0 = v_{GS2} + v_S \end{cases} \Rightarrow \boxed{v_{id} == \left(v_{GS1} - v_{GS2}\right)}$$

$$v_o = v_{D2} - v_{D1} = \left(V_{DD} - R_D i_{D2}\right) - \left(V_{DD} - R_D i_{D1}\right)$$

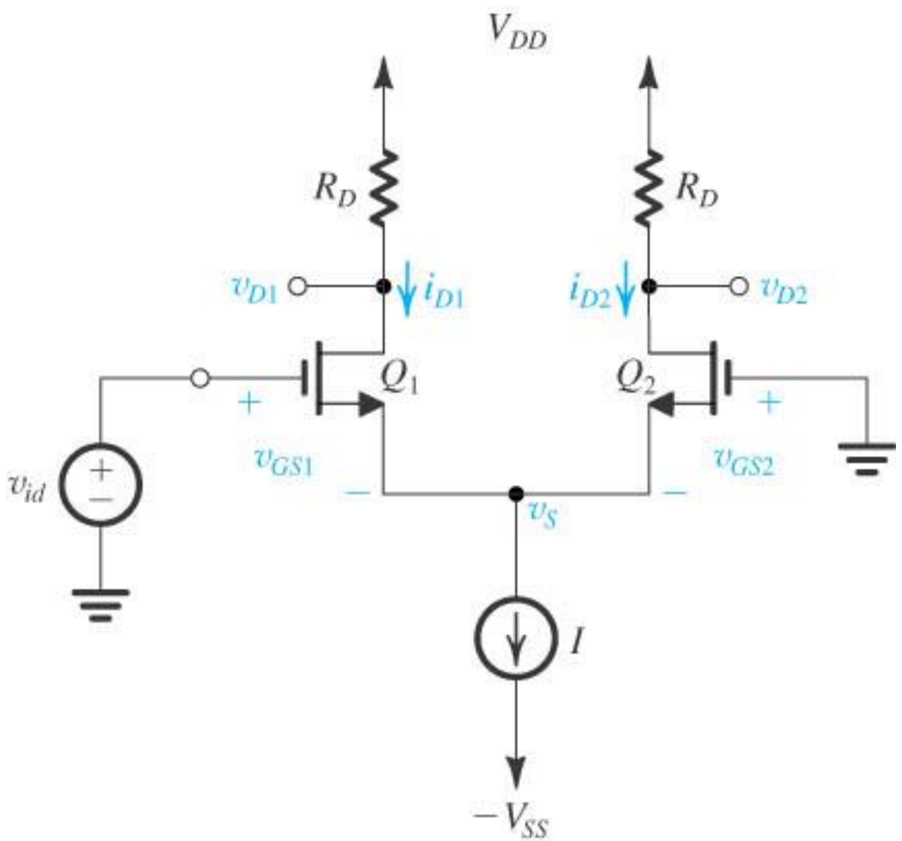
$$\Rightarrow i_{D1} - i_{D2} = \frac{v_o}{R_D}$$

$$i_{D1} + i_{D2} = I$$

$$\Rightarrow \boxed{\begin{cases} i_{d1} = \dfrac{I_0}{2} + \dfrac{v_o}{2R_d} \\ i_{d2} = \dfrac{I_0}{2} - \dfrac{v_o}{2R_d} \end{cases}}$$

Ideal MOS differential pair

Differential input voltage: large-signal behavior



$$\begin{cases} i_{D1} = \frac{1}{2} k_n' \frac{W}{L} \left(v_{GS1} - V_t\right)^2 \\ i_{D2} = \frac{1}{2} k_n' \frac{W}{L} \left(v_{GS2} - V_t\right)^2 \end{cases}$$

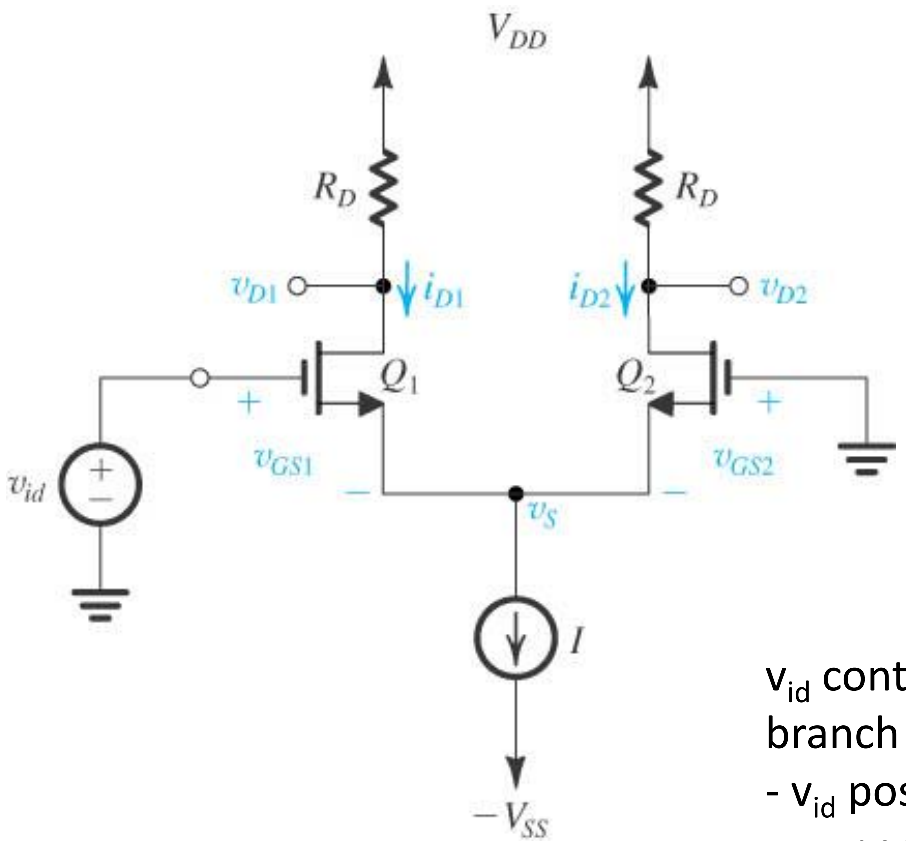
$$\Rightarrow \quad \underbrace{v_{GS1} - v_{GS2}}_{=v_{id}} = \sqrt{\frac{2}{k_n'} \frac{L}{W}} \left(\sqrt{i_{D1}} - \sqrt{i_{D2}}\right)$$

$$\begin{cases} i_{D1} = \frac{I}{2} + \frac{v_o}{2R_D} \\ i_{D2} = \frac{I}{2} - \frac{v_o}{2R_D} \end{cases}$$

$$\boxed{v_o = R_D v_{id} \sqrt{k_n' \frac{W}{L} I} \sqrt{1 - \frac{1}{2} k_n' \frac{W}{L} \frac{v_{id}^2}{2I}}}$$

Ideal MOS differential pair

Differential input voltage: large-signal behavior



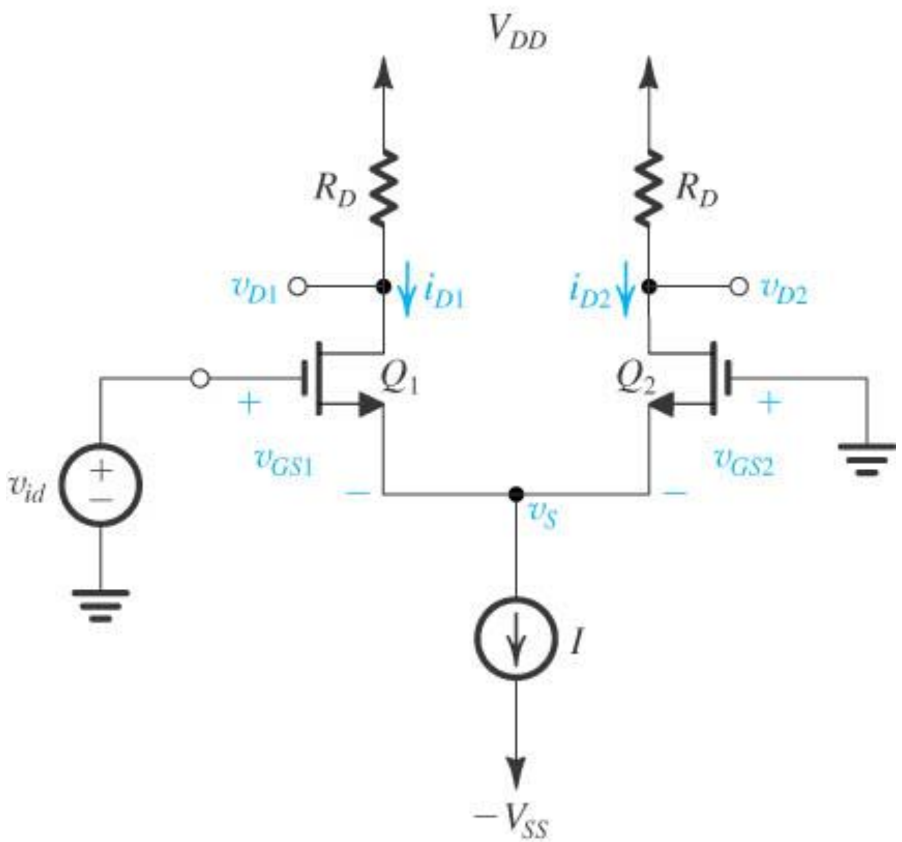
$$v_o = R_D v_{id} \sqrt{k_n' \frac{W}{L} I} \sqrt{1 - \frac{1}{2} k_n' \frac{W}{L} \frac{v_{id}^2}{2I}}$$

$$\Rightarrow \begin{cases} i_{D1} = \dfrac{I}{2} + \sqrt{k_n' \dfrac{W}{L} I} \left(\dfrac{v_{id}}{2} \right) \sqrt{1 - \dfrac{(v_{id}/2)^2}{1/k_n' \dfrac{W}{L}}} \\ i_{D2} = \dfrac{I}{2} - \sqrt{k_n' \dfrac{W}{L} I} \left(\dfrac{v_{id}}{2} \right) \sqrt{1 - \dfrac{(v_{id}/2)^2}{1/k_n' \dfrac{W}{L}}} \end{cases}$$

v_{id} controls how much current flows through each branch of the circuit
- v_{id} positive: more current through left branch
- v_{id} negative: more current through right branch

Ideal MOS differential pair

Differential input voltage: large-signal behavior



Note that when $v_{id} = 0$:

$$i_{D1} = i_{D2} = I/2$$

$$v_{GS1} = v_{GS2} = V_{GS}$$

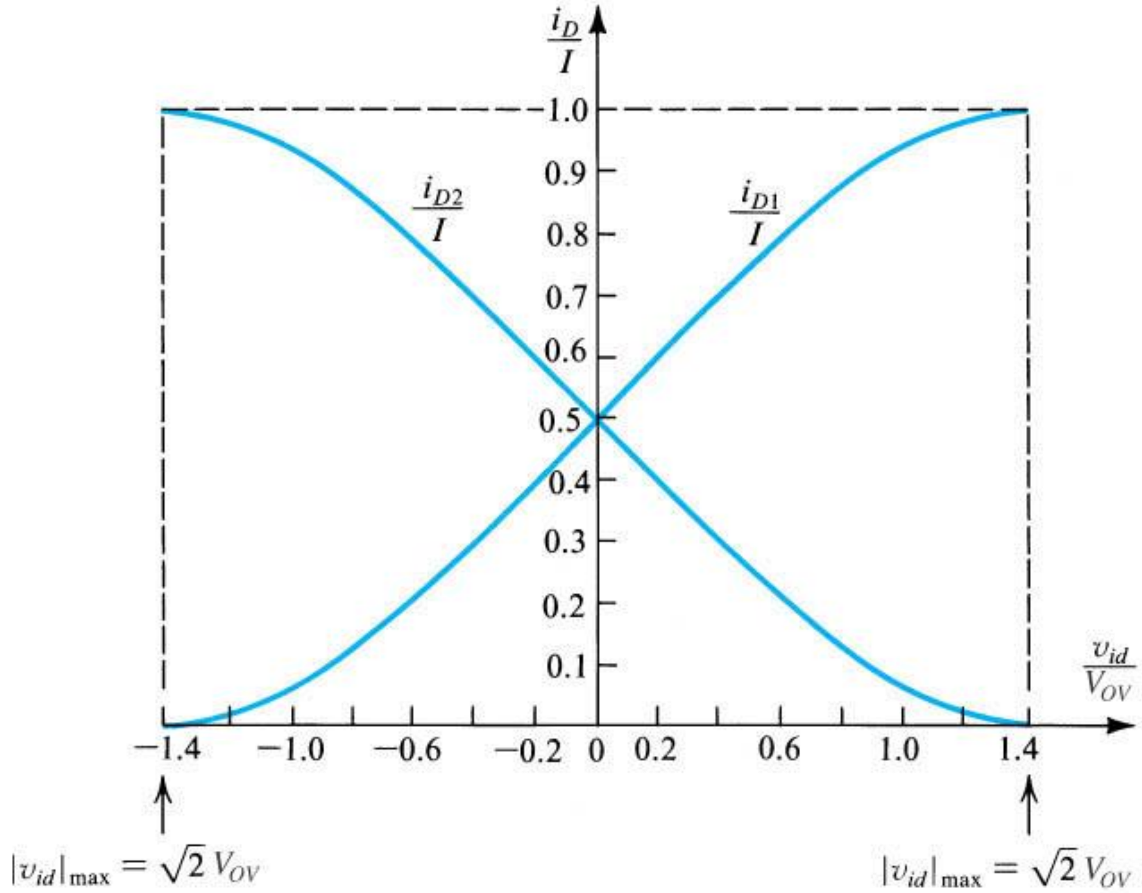
$$\Rightarrow \frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} \underbrace{\left(V_{GS} - V_t\right)}_{=V_{OV}}^2$$

$$\Rightarrow \begin{cases} i_{D1} = \dfrac{I}{2} + \left(\dfrac{I}{V_{OV}}\right)\dfrac{v_{id}}{2}\sqrt{1-\left(\dfrac{v_{id}/2}{V_{OV}}\right)^2} \\ i_{D2} = \dfrac{I}{2} - \left(\dfrac{I}{V_{OV}}\right)\dfrac{v_{id}}{2}\sqrt{1-\left(\dfrac{v_{id}/2}{V_{OV}}\right)^2} \end{cases}$$

Ideal MOS differential pair

Differential input voltage: large-signal behavior

- currents i_{D1} and i_{D2}



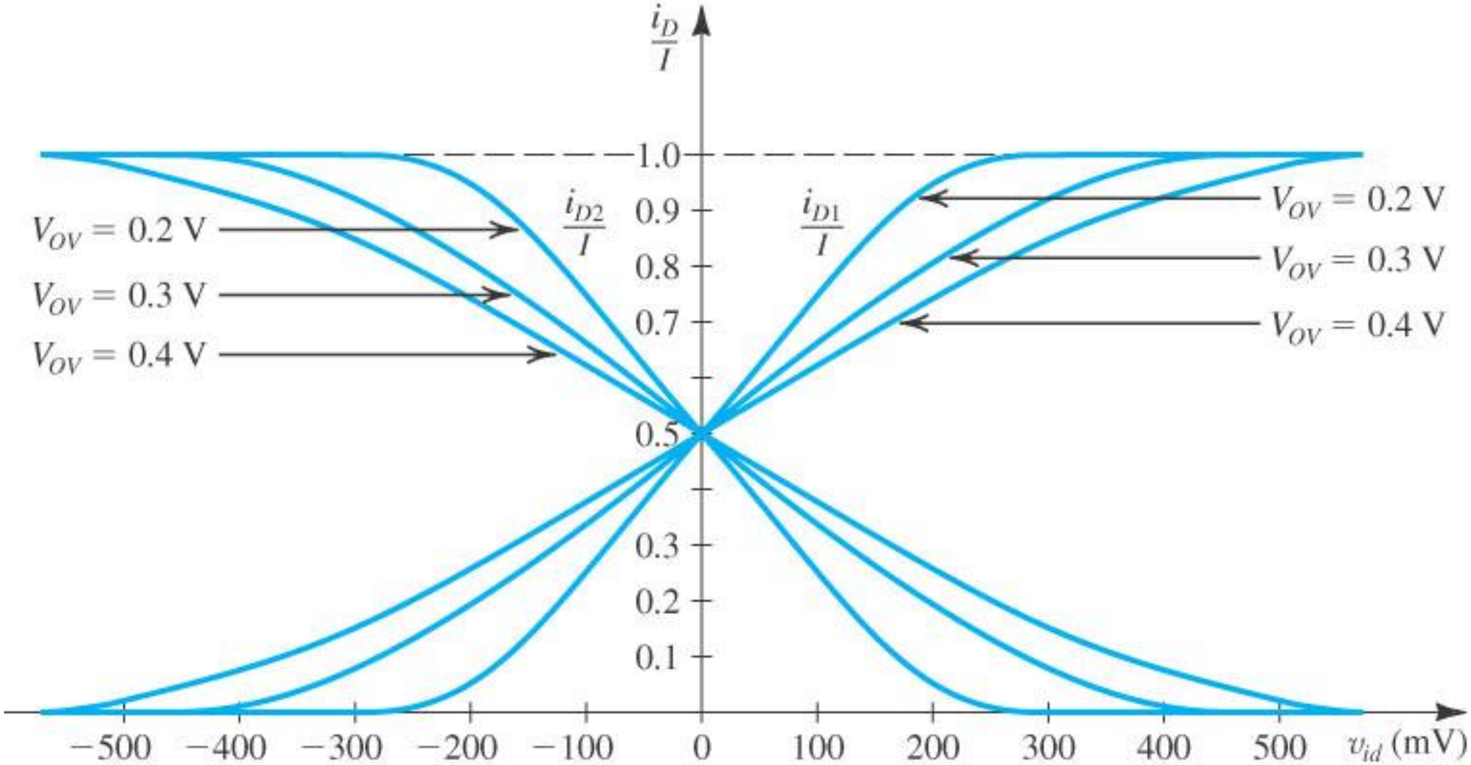
Ideal MOS differential pair

Differential input voltage: large-signal behavior

- V_{OV} can be changed (e.g. by changing W or L for unchanged I)

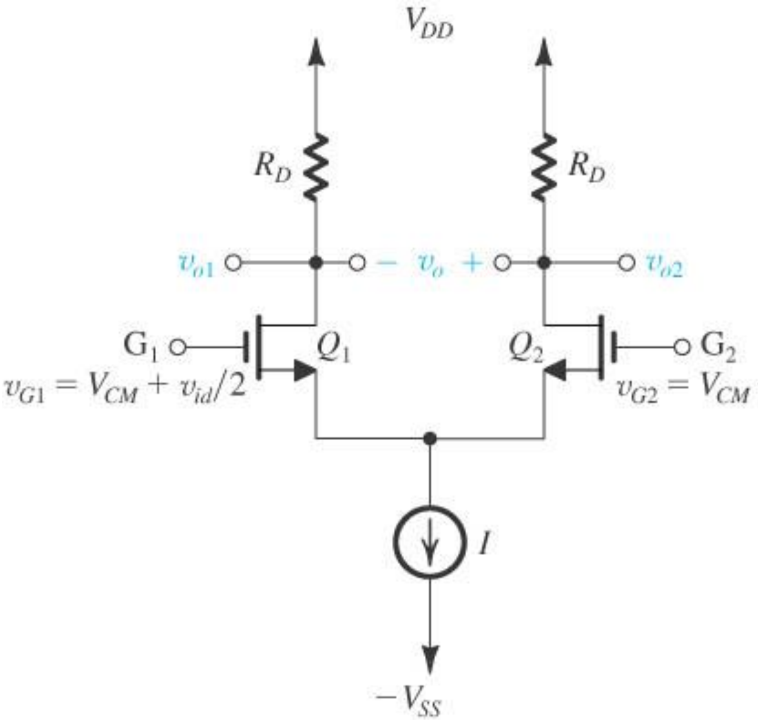
$$\frac{I}{2} = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^{\ 2}$$

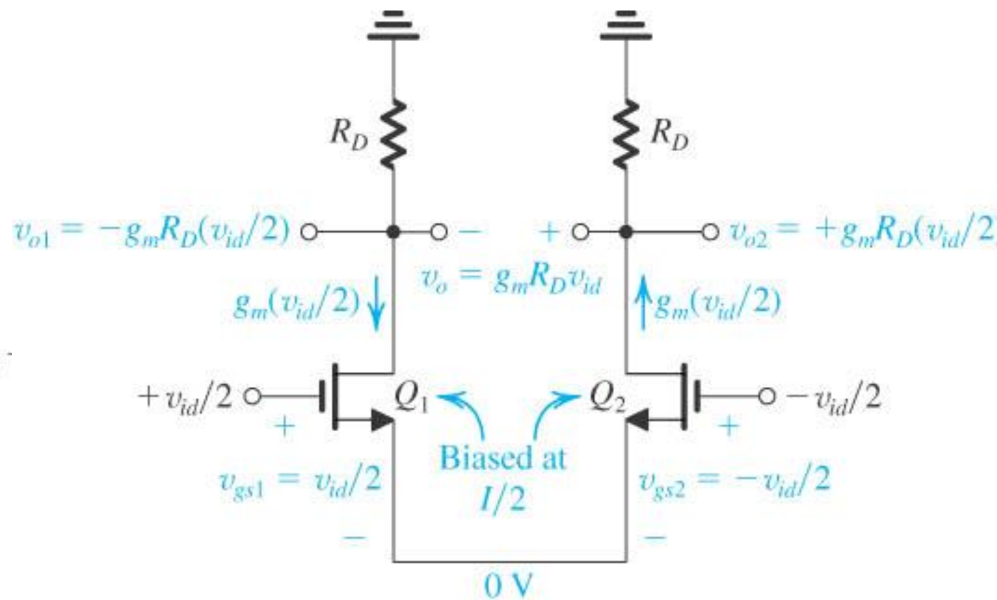
$\Rightarrow$ Controls slope of currents



Ideal MOS differential pair

Differential input: small-signal behavior





$$\begin{cases} v_{G1} = v_{CM} + \dfrac{v_{id}}{2} \\ v_{G2} = v_{CM} - \dfrac{v_{id}}{2} \end{cases}$$

$$\begin{cases} v_{o1} = -R_D i_{d1} = -R_D g_m v_{gs1} \\ v_{o2} = -R_D i_{d2} = -R_D g_m v_{gs2} \end{cases}$$

$$\Rightarrow \boxed{v_o = g_m R_D v_{id}}$$

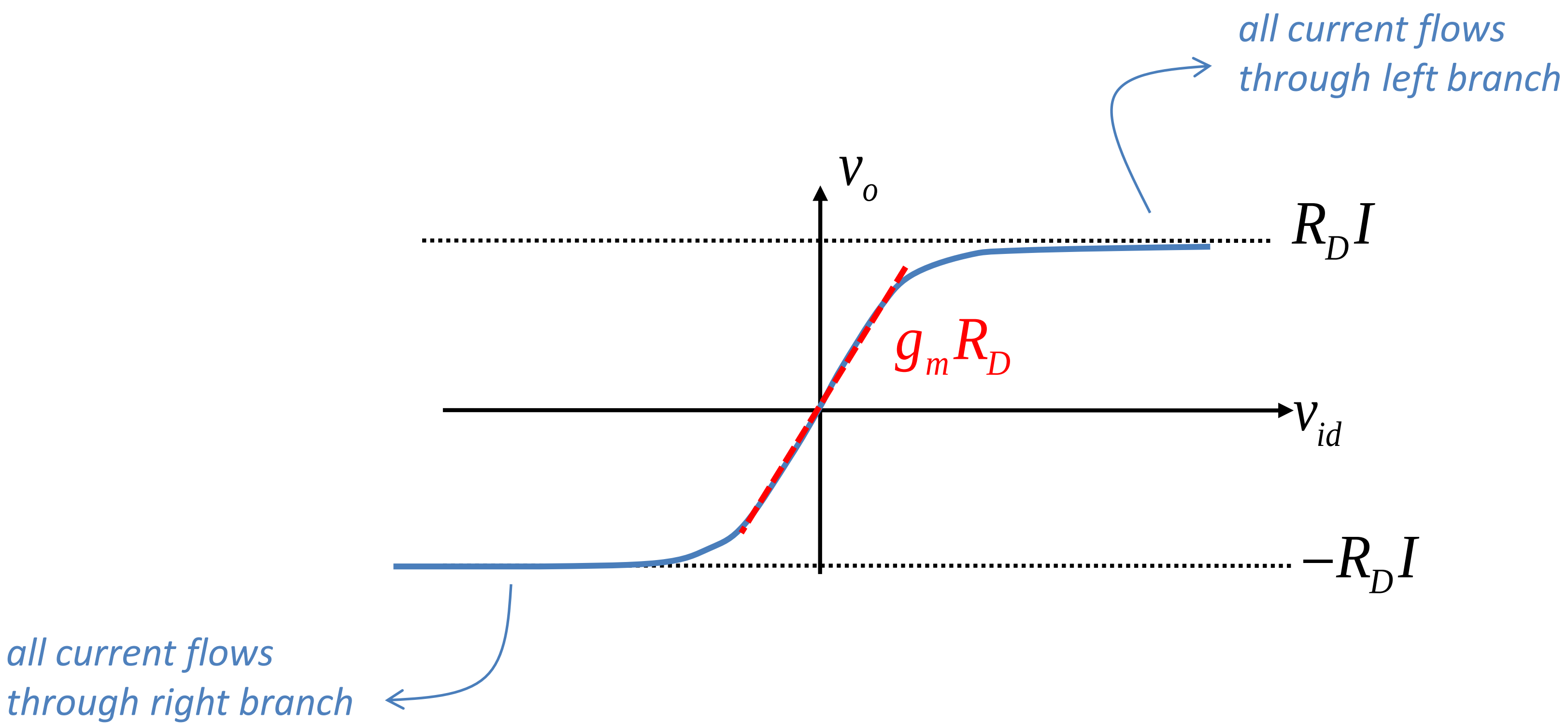
Ideal MOS differential pair

Differential input: small-signal behavior

$$v_o = g_m R_D v_{id}$$

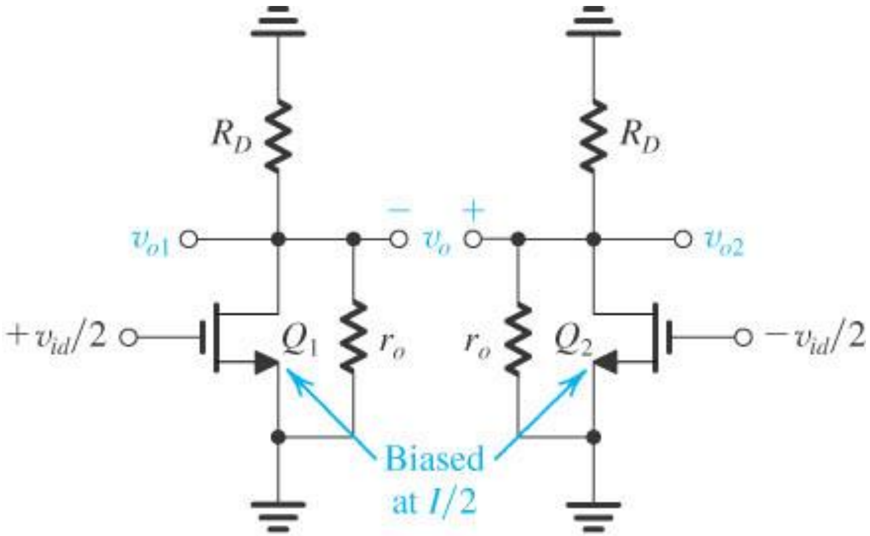
$$\boxed{\Rightarrow A_d = g_m R_D}$$

$$\text{with } g_m = \frac{I}{V_{GS} - V_t} = \frac{I}{V_{OV}}$$



Ideal MOS differential pair

effect of MOSFET's r_o



$$v_{o1} = -g_m \left(R_D \parallel r_o\right)\left(v_{id} / 2\right)$$

$$v_{o2} = +g_m \left(R_D \parallel r_o\right)\left(v_{id} / 2\right)$$

$$\Rightarrow v_o = g_m \left(R_D \parallel r_o\right) v_{id}$$

- NMOS output resistance plays role in final gain
- Resistance of current source for biasing plays no role in gain

$\Rightarrow$ *prove this as an exercise!*

Nonidealities of MOS differential pair

Common-mode rejection ratio

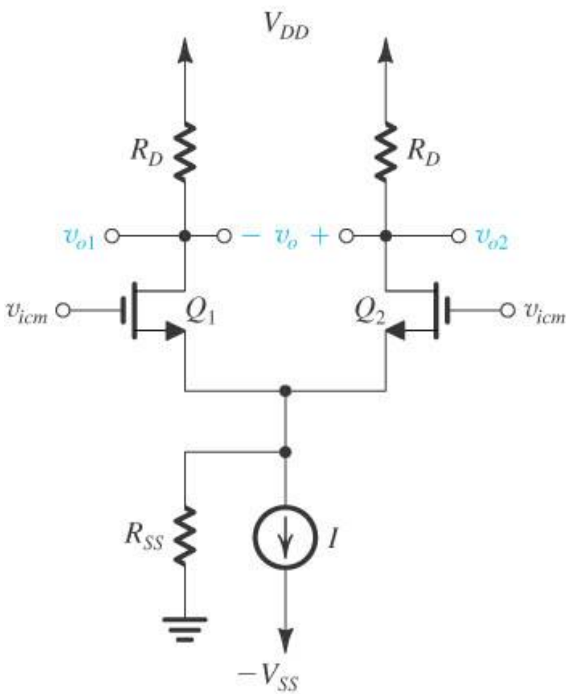
$$\text{CMRR} = \left|\frac{A_d}{A_{cm}}\right|$$

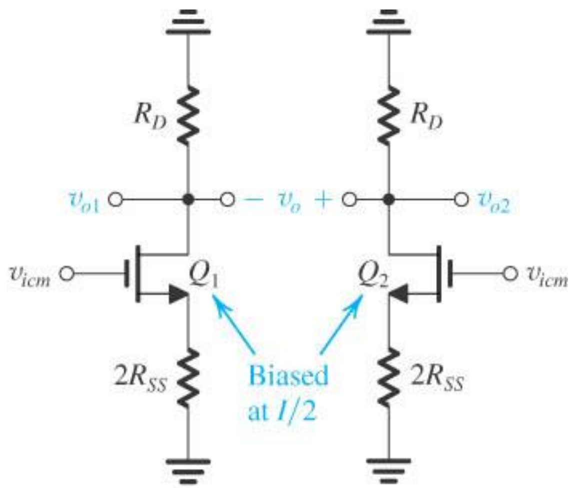
- For a ideal MOS differential pair:

$$A_{cm} = \frac{v_{o2} - v_{o1}}{v_{icm}} = 0$$

$$A_d = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

$$\Rightarrow \text{CMRR} = \infty$$





Nonidealities of MOS differential pair

Effect of R_D mismatch

- Q1 has load R_D and Q2 has load $R_D + \Delta R_D$

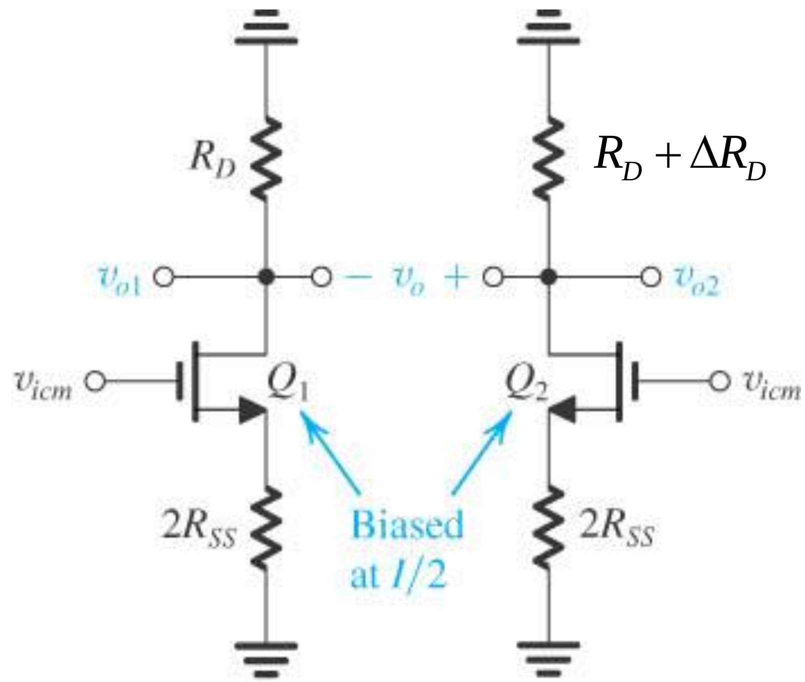
- $$v_{o1} \cong -\frac{R_D}{2R_{SS}} v_{icm}$$

$$v_{o2} \cong -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$$

$$\Rightarrow A_{cm} = -\frac{\Delta R_D}{2R_{SS}} \qquad A_d = g_m R_D$$

$$\text{CMRR} = \frac{g_m R_D}{\Delta R_D / 2R_{SS}}$$

$$\Rightarrow \boxed{\text{CMRR} = \frac{2 g_m R_{SS}}{\left(\Delta R_D / R_D\right)}}$$



Nonidealities of MOS differential pair

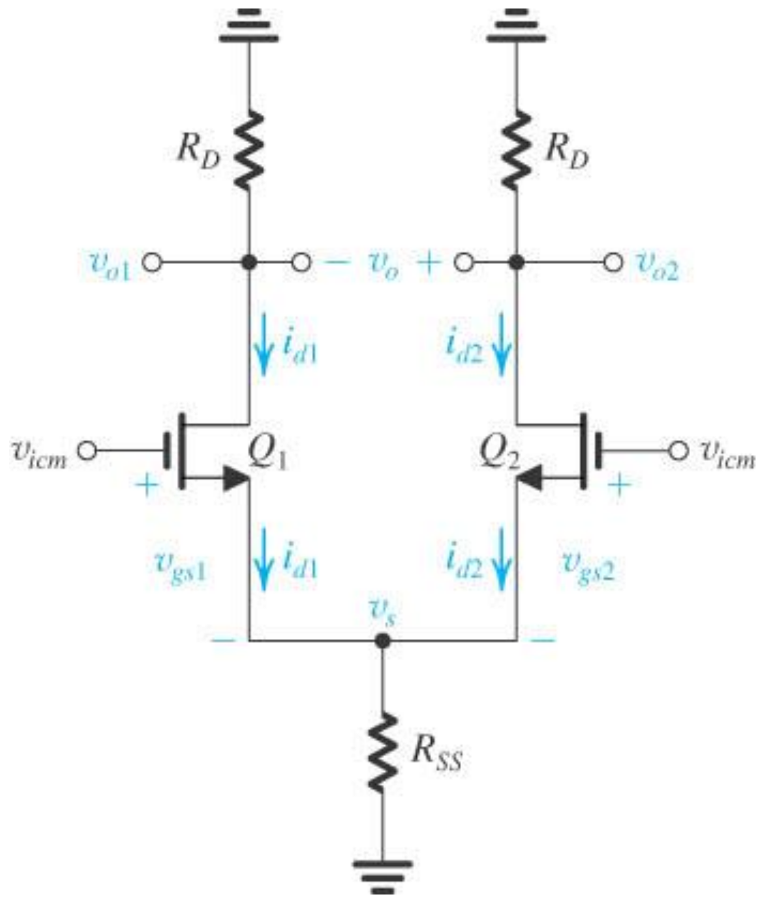
Effect of g_m mismatch

$$\begin{cases} i_{d1} = g_{m1} v_{gs1} \\ i_{d2} = g_{m2} v_{gs2} \end{cases} \Rightarrow \frac{i_{d1}}{i_{d2}} = \frac{g_{m1}}{g_{m2}}$$

$$i_{d1} + i_{d2} = \frac{v_S}{R_{SS}} \qquad R_{SS} \text{ large} \Rightarrow v_S \cong v_{icm}$$

$$\Rightarrow i_{d1} + i_{d2} \cong \frac{v_{icm}}{R_{SS}}$$

$$\Rightarrow \begin{cases} i_{d1} = \dfrac{g_{m1} v_{icm}}{\left(g_{m1} + g_{m2}\right) R_{SS}} \\ i_{d2} = \dfrac{g_{m2} v_{icm}}{\left(g_{m1} + g_{m2}\right) R_{SS}} \end{cases}$$



Nonidealities of MOS differential pair

Effect of g_m mismatch

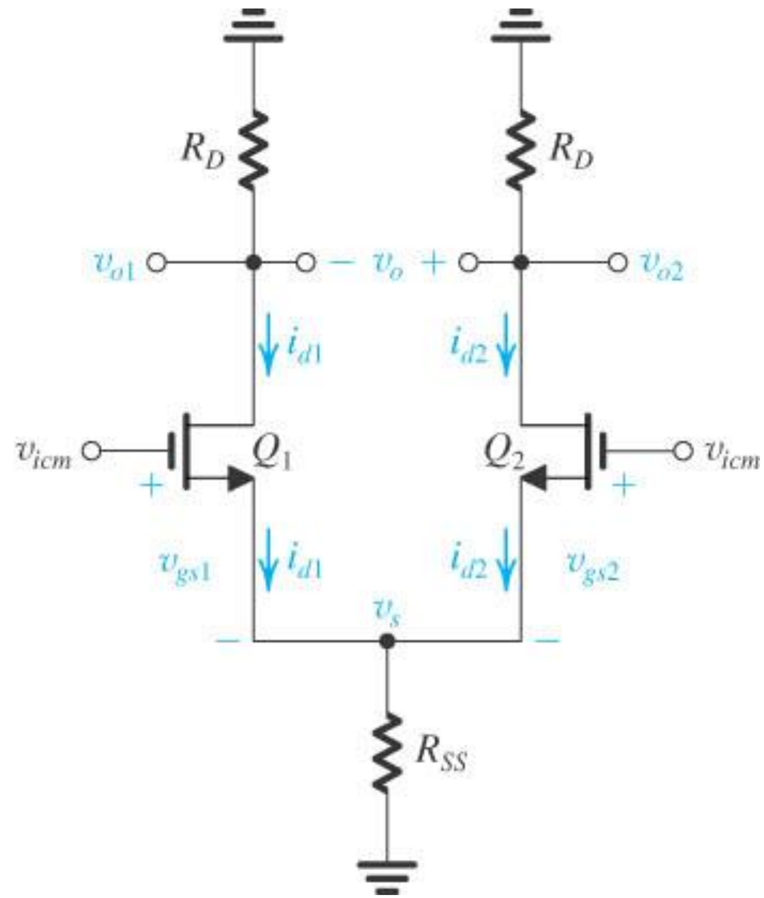
$$\Delta g_m \text{ small} \Rightarrow \begin{cases} g_{m1} + g_{m2} \cong 2g_m \\ g_{m1} + g_{m2} = \Delta g_m \end{cases}$$

$$\Rightarrow \begin{cases} i_{d1} = \dfrac{g_{m1} v_{icm}}{2g_m R_{SS}} \\[2ex] i_{d2} = \dfrac{g_{m2} v_{icm}}{2g_m R_{SS}} \end{cases}$$

$$\Rightarrow v_o = v_{o2} - v_{o1} = -i_{d2} R_D + i_{d1} R_D$$

$$\Rightarrow v_o = \frac{\Delta g_m R_D}{2g_m R_{SS}} v_{icm}$$

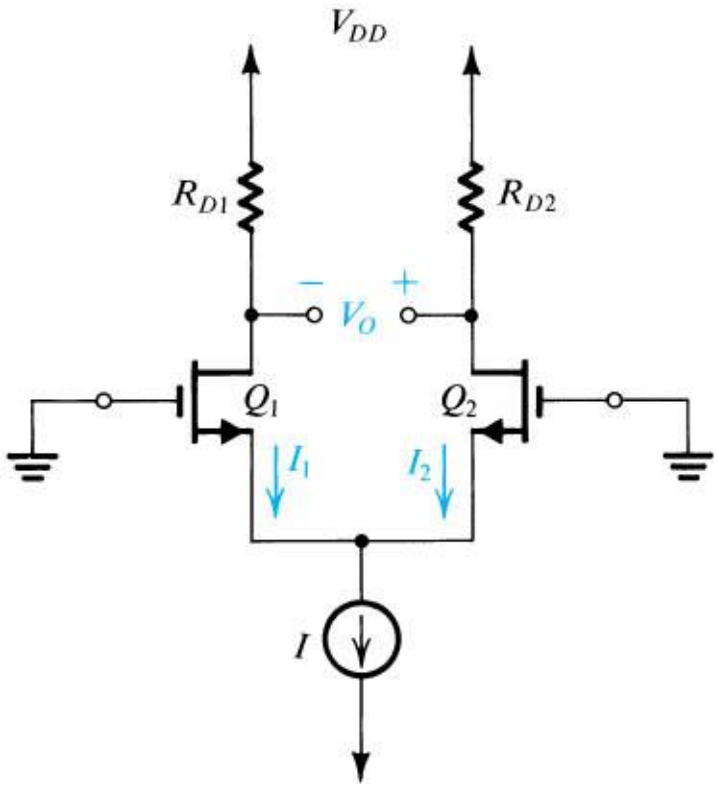
$$\Rightarrow \boxed{\text{CMRR} = \frac{2g_m R_{SS}}{(\Delta g_m / g_m)}}$$

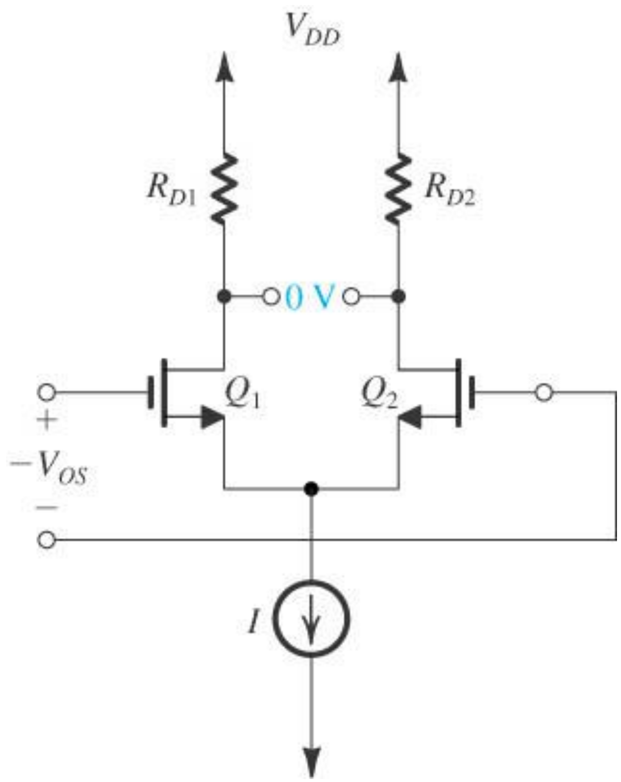


Nonidealities: input offset voltage

Mismatches in circuit cause output offset voltage

- Imagine both inputs grounded
  - $\Rightarrow$ Nonidealities will cause output offset voltage V_O
  - $\Rightarrow$ We divide V_O by A_d to get input offset voltage V_{OS}

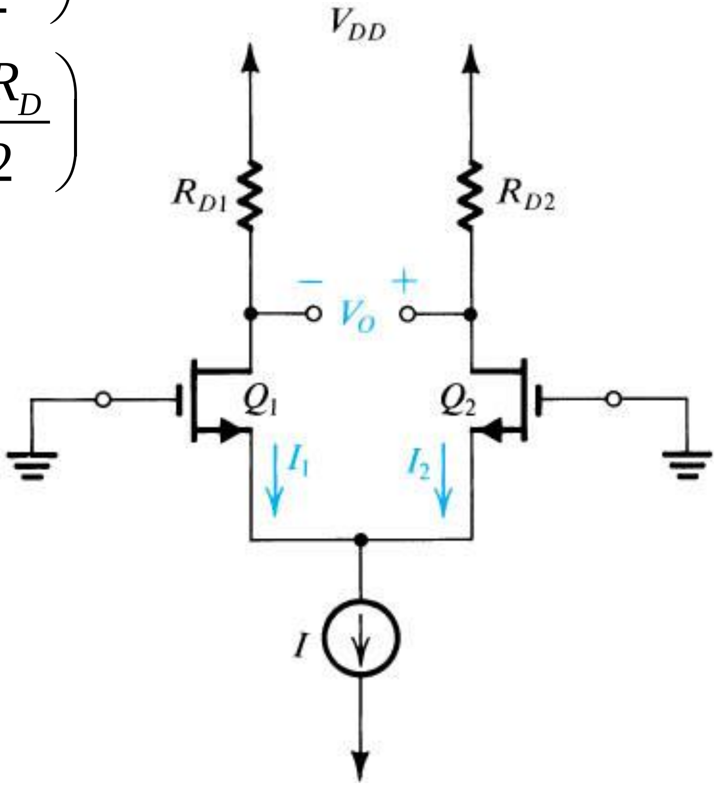




Nonidealities: input offset voltage

Effect of R_D mismatch on V_{OS}

$$\begin{cases} R_{D1} = R_D + \dfrac{\Delta R_D}{2} \\ R_{D2} = R_D - \dfrac{\Delta R_D}{2} \end{cases} \Rightarrow \begin{cases} V_{D1} = V_{DD} - I_D\left(R_D + \dfrac{\Delta R_D}{2}\right) \\ V_{D2} = V_{DD} - I_D\left(R_D - \dfrac{\Delta R_D}{2}\right) \end{cases}$$



$$\Rightarrow V_O = V_{D2} - V_{D1} = \frac{I}{2}\Delta R_D$$

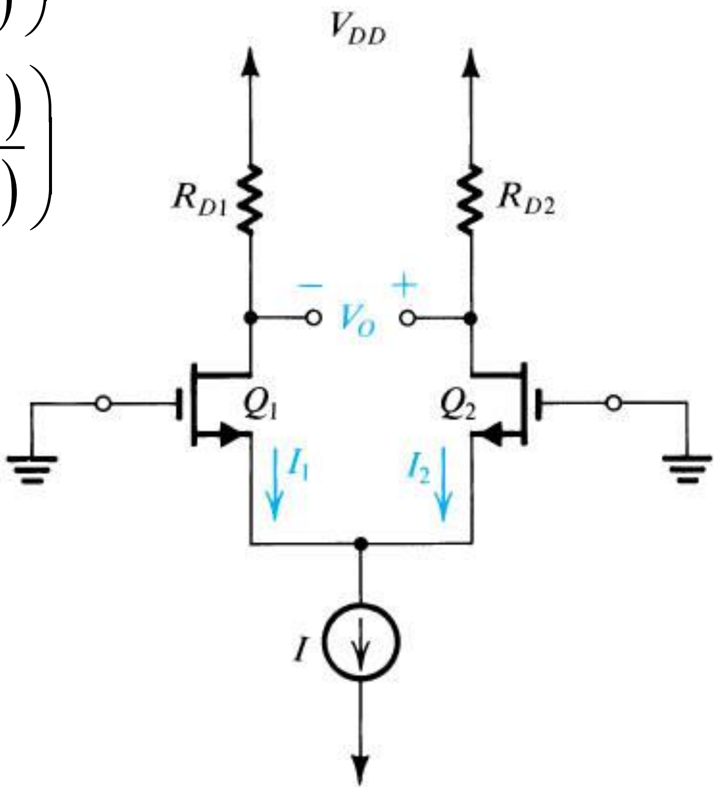
$V_{OS} = V_O / A_d$

$$\Rightarrow V_{OS} = \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta R_D}{R_D}\right)$$

Nonidealities: input offset voltage

Effect of (W/L) mismatch on V_{OS}

$$\begin{cases} \left(\frac{W}{L}\right)_1 = \frac{W}{L} + \frac{1}{2}\Delta\left(\frac{W}{L}\right) \\ \left(\frac{W}{L}\right)_2 = \frac{W}{L} - \frac{1}{2}\Delta\left(\frac{W}{L}\right) \end{cases} \Rightarrow \begin{cases} I_1 = \frac{I}{2} + \frac{I}{2}\left(\frac{\Delta(W/L)}{2(W/L)}\right) \\ I_2 = \frac{I}{2} - \frac{I}{2}\left(\frac{\Delta(W/L)}{2(W/L)}\right) \end{cases}$$



$$\Rightarrow V_O = R_D\left(I_1 - I_2\right)$$

$$\Rightarrow V_{OS} = \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta(W/L)}{(W/L)}\right)$$

Nonidealities: input offset voltage

Effect of V_t mismatch on V_{OS}

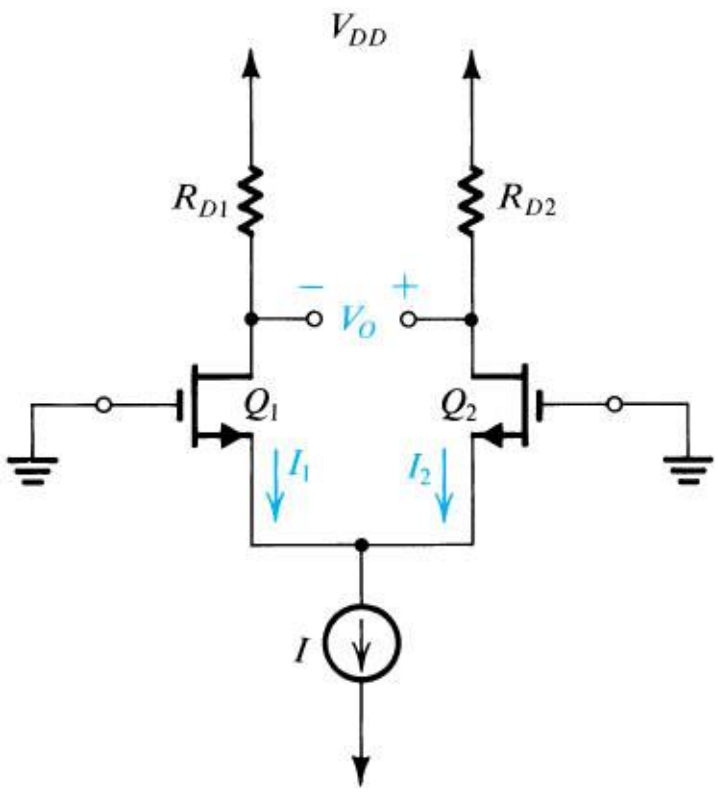
$$\begin{cases} V_{t1} = V_t + \dfrac{\Delta V_t}{2} \\ V_{t2} = V_t - \dfrac{\Delta V_t}{2} \end{cases}$$

$$I_1 = \frac{1}{2} k_n' \frac{W}{L} \left(V_{GS} - V_t - \frac{\Delta V_t}{2} \right)^2$$

$$= \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \left[1 - \frac{\Delta V_t}{2(V_{GS} - V_t)} \right]^2$$

$$\approx \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \left(1 - \frac{\Delta V_t}{(V_{GS} - V_t)} \right)$$

$$I_2 \approx \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_t)^2 \left(1 + \frac{\Delta V_t}{(V_{GS} - V_t)} \right)$$



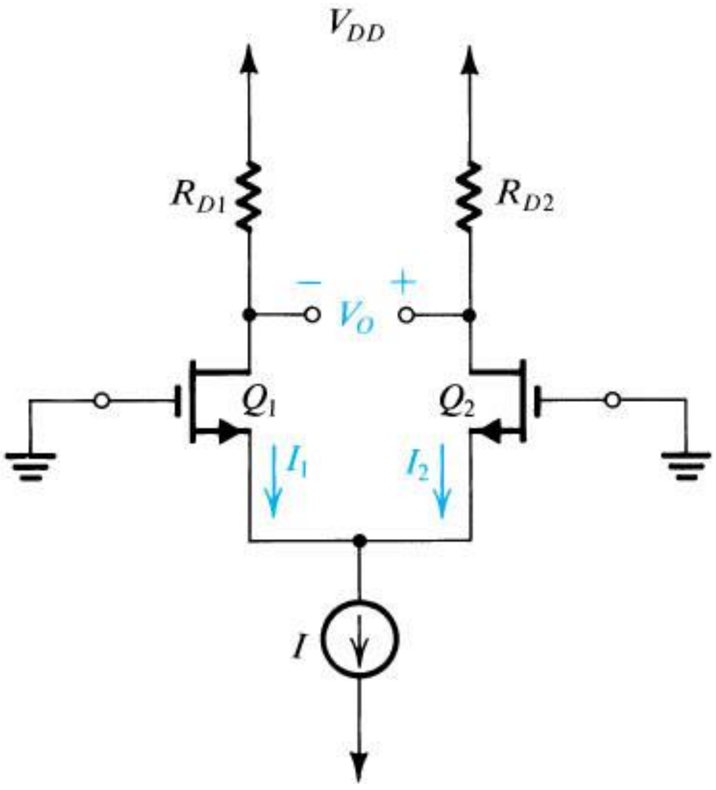
Nonidealities: input offset voltage

Effect of V_t mismatch on V_{OS}

$$\Rightarrow V_O = R_D\left(I_1 - I_2\right)$$

$$\Rightarrow V_O = -R_D I \frac{\Delta V_t}{V_{OV}}$$

$$\Rightarrow V_{OS} = \Delta V_t$$



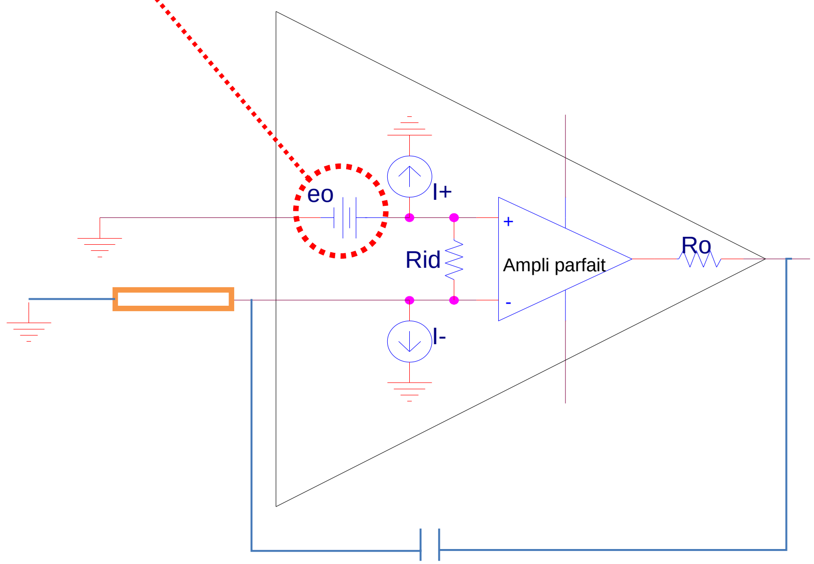
Nonidealities: input offset voltage

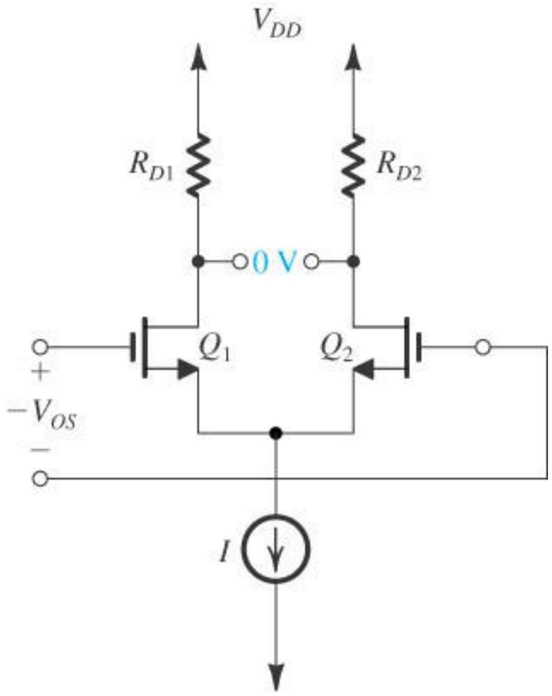
Combined effect of mismatches on V_{OS}

- Circuit is linear and three sources of offset voltage are uncorrelated

  $\Rightarrow$ superposition can be applied

$$V_{OS} = \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta R_D}{R_D}\right) + \left(\frac{V_{OV}}{2}\right)\left(\frac{\Delta(W/L)}{(W/L)}\right) + \Delta V_t$$





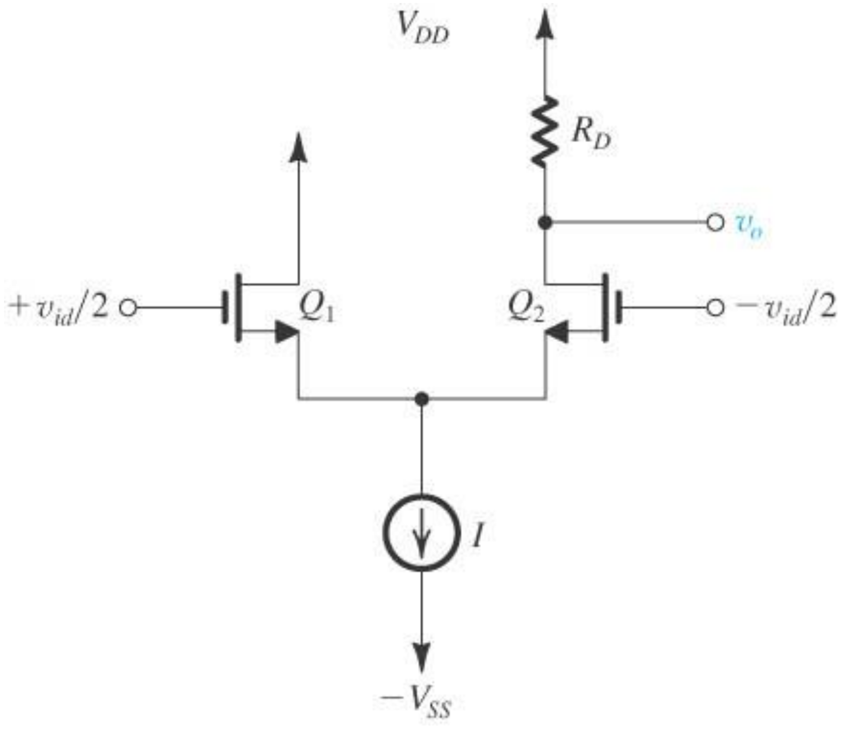
$\Rightarrow$ Input offset voltage in op-amp is due to assymetries in NMOS differential pair

Differential amplifier with active load

Differential to single-ended conversion

- Mulitstage circuits usually use single-ended voltages
  - Voltage w.r.t. ground of circuit

  $\Rightarrow$ Differential output cannot always be used



$$v_o = g_m R_D \frac{v_{id}}{2}$$

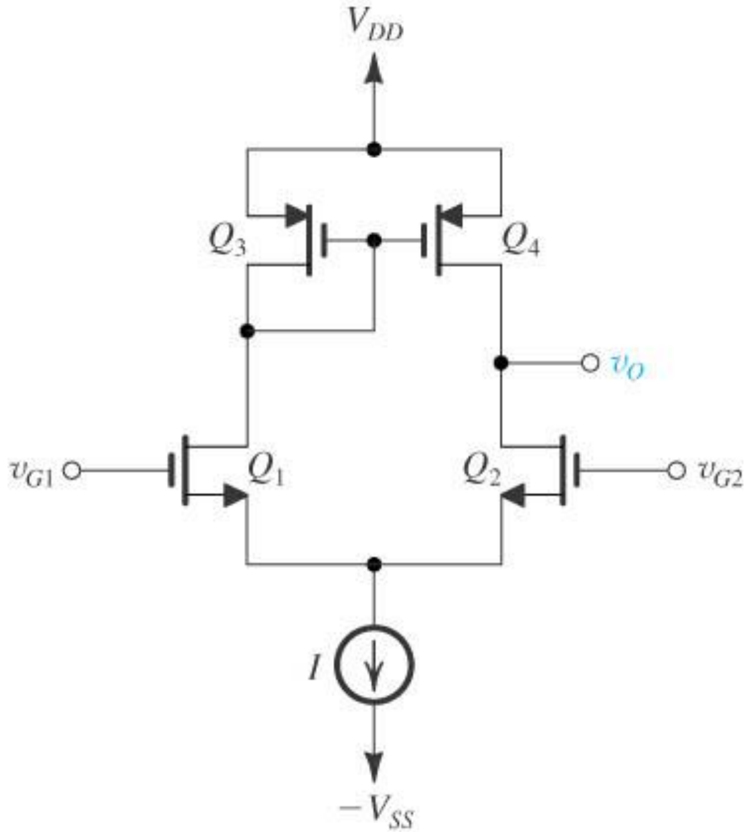
$\Rightarrow$we lose a factor 2 (6dB)

$\Rightarrow$ « wasting » the signal

Differential amplifier with active load

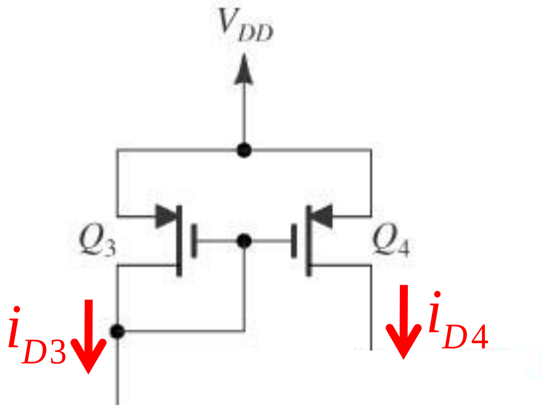
Active-loaded differential MOS pair

- differential pair Q1 and Q2 loaded in a PMOS current mirror by Q3 and Q4



Reminder

PMOS current mirror



- Current through Q3 determines current going through Q4

$$\text{Q3 saturation} \Leftrightarrow v_{SD3} \geq v_{SG3} - V_t$$
$$\Leftrightarrow v_{D3} \geq v_{G3} - V_t$$
$$\Leftrightarrow 0 \geq -V_t$$

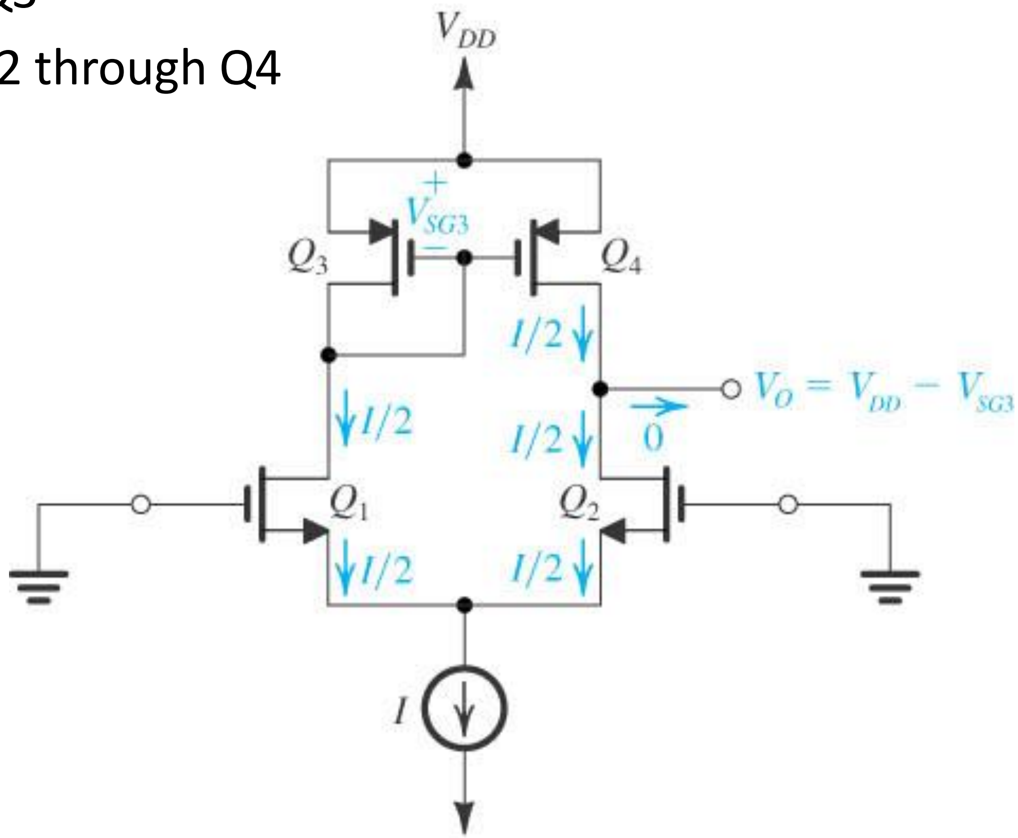
$$\Rightarrow \text{Q3 always in saturation region}$$

$$i_{D3} = \frac{1}{2} k_n' \frac{W}{L} \left(v_{SG3} - V_t \right)^2$$
$$= \frac{1}{2} k_n' \frac{W}{L} \left(v_{SG4} - V_t \right)^2$$
$$\boxed{\Rightarrow i_{D3} = i_{D4}}$$

Differential amplifier with active load

Active-loaded differential MOS pair

- Q1 and Q2 have same common-mode voltage
  - $\Rightarrow$ current I/2 flowing through Q1 and Q2
  - $\Rightarrow$ current I/2 flowing throug Q3
  - $\Rightarrow$ mirror current => current I/2 through Q4
  - $\Rightarrow$ output current is zero
  - $\Rightarrow$ equilibrium state



Differential amplifier with active load

Active-loaded differential MOS pair

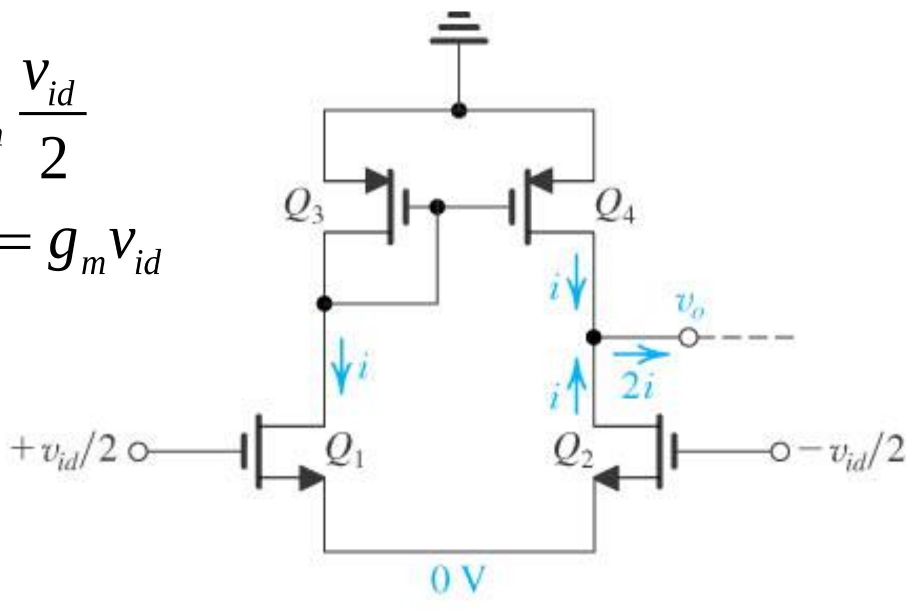
- Differential voltage causes
  - increase of i in Q1 and decrease of i in Q2
  - current i going through Q3

  $\Rightarrow$ current i going through Q4

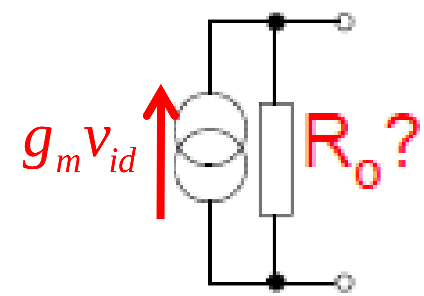
  $\Rightarrow$ output current of 2i

$$i = g_m \frac{v_{id}}{2}$$

$$\Rightarrow 2i = g_m v_{id}$$



Norton equivalent circuit:



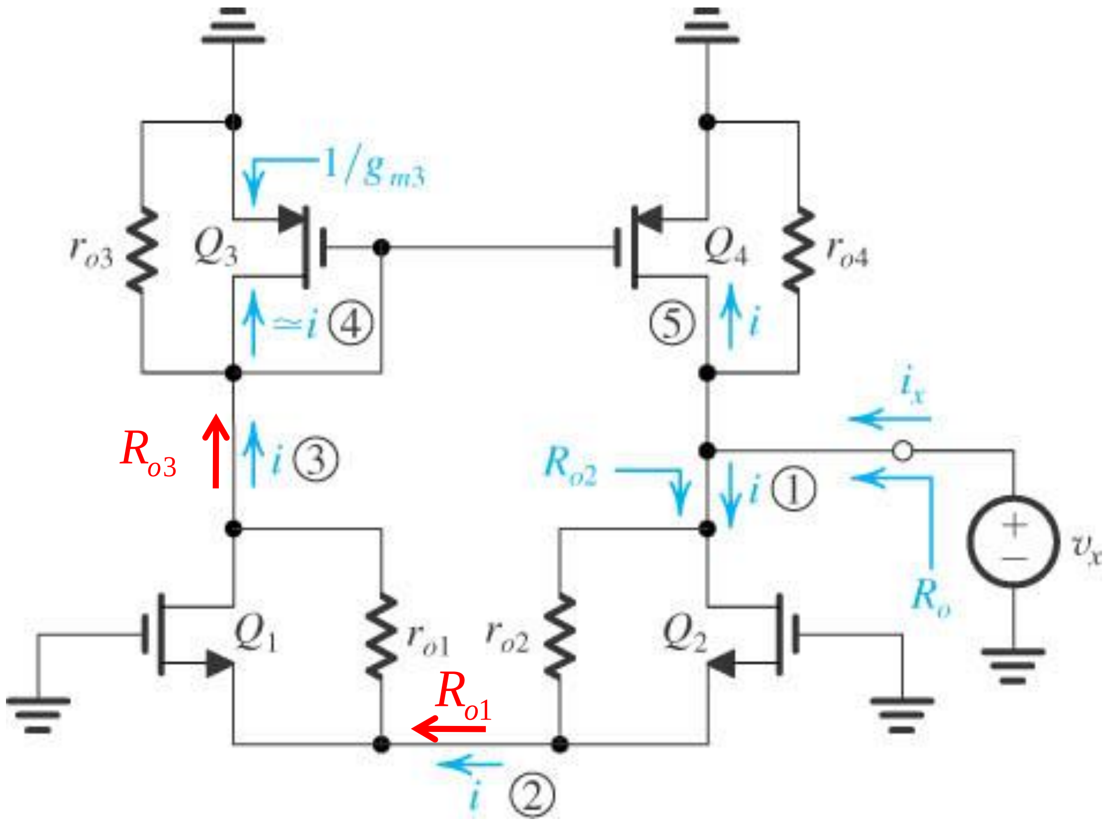
$$v_o = R_o g_m v_{id}$$

$$\Rightarrow A_d = R_o g_m$$

Differential amplifier with active load

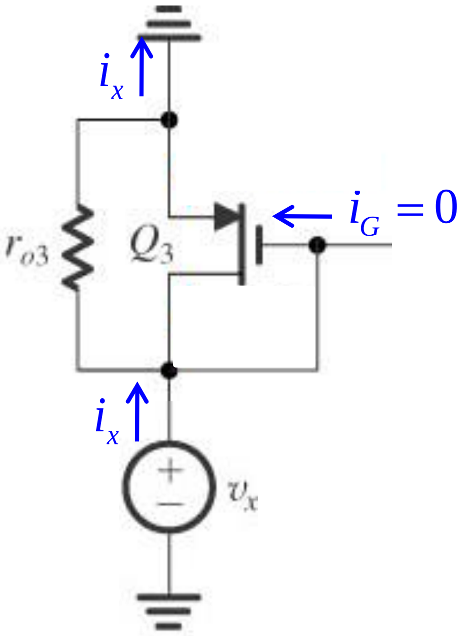
Output resistance R_o

- Many intermediate steps…



Differential amplifier with active load

Output resistance R_o – step 1: compute R_{O3}



$$v_x = r_{o3}\left(i_x + g_{m3} v_{SG3}\right)$$

$$v_{SG3} = 0 - v_x$$

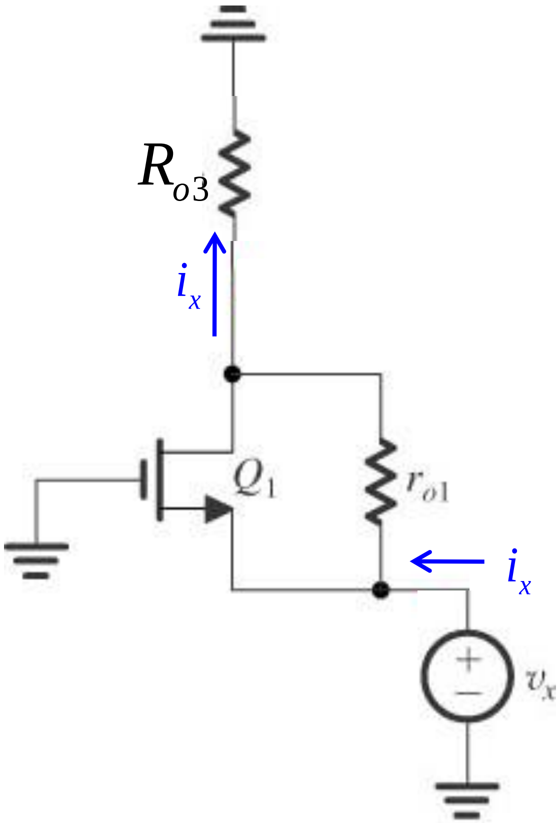
$$v_x = r_{o3}\left(i_x - g_{m3} v_x\right)$$

$$\Rightarrow R_{o3} = \frac{v_x}{i_x} = \frac{r_{o3}}{1 + r_{o3} g_{m3}}$$

$$\Rightarrow R_{o3} \approx \frac{1}{g_{m3}}$$

Differential amplifier with active load

Output resistance R_o – step 2: compute R_{O1}



$$v_x = R_{o3} i_x + r_{o1}\left(i_x + g_{m1} v_{GS1}\right)$$

$$v_{SG3} = 0 - v_x$$

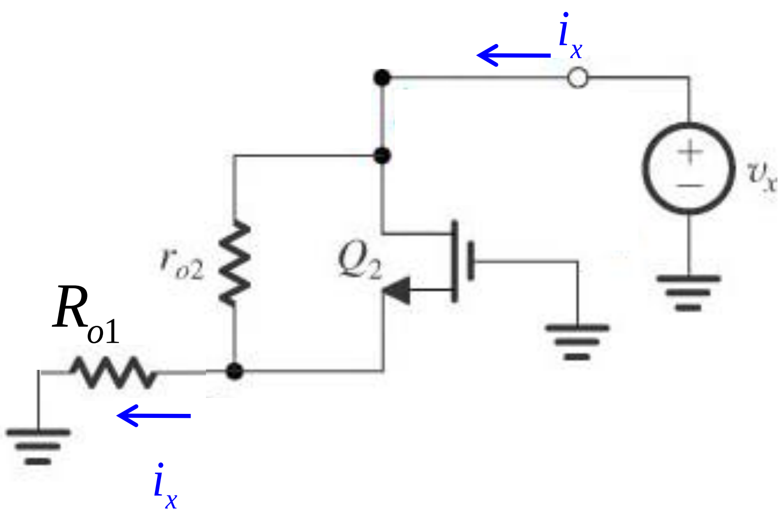
$$v_x = R_{o3} i_x + r_{o1}\left(i_x - g_{m1} v_x\right)$$

$$\Rightarrow R_{o1} = \frac{v_x}{i_x} = \frac{R_{o3} + r_{o1}}{1 + r_{o1} g_{m1}} = \frac{1/g_{m3} + r_{o1}}{1 + r_{o1} g_{m1}}$$

$$\Rightarrow R_{o1} \approx \frac{1}{g_{m1}}$$

Differential amplifier with active load

Output resistance R_o – step 3: compute R_{O2}



$$v_x = R_{o1} i_x + r_{o2}\left(i_x - g_{m2} v_{GS2}\right)$$

$$\Downarrow \quad v_{GS2} = 0 - v_S = 0 - R_{o1} i_x$$

$$v_x = R_{o1} i_x + r_{o2}\left(i_x + g_{m2} R_{o1} i_x\right)$$

$$\Rightarrow R_{o2} = \frac{v_x}{i_x} = R_{o1} + r_{o2} + r_{o2} g_{m2} R_{o1}$$

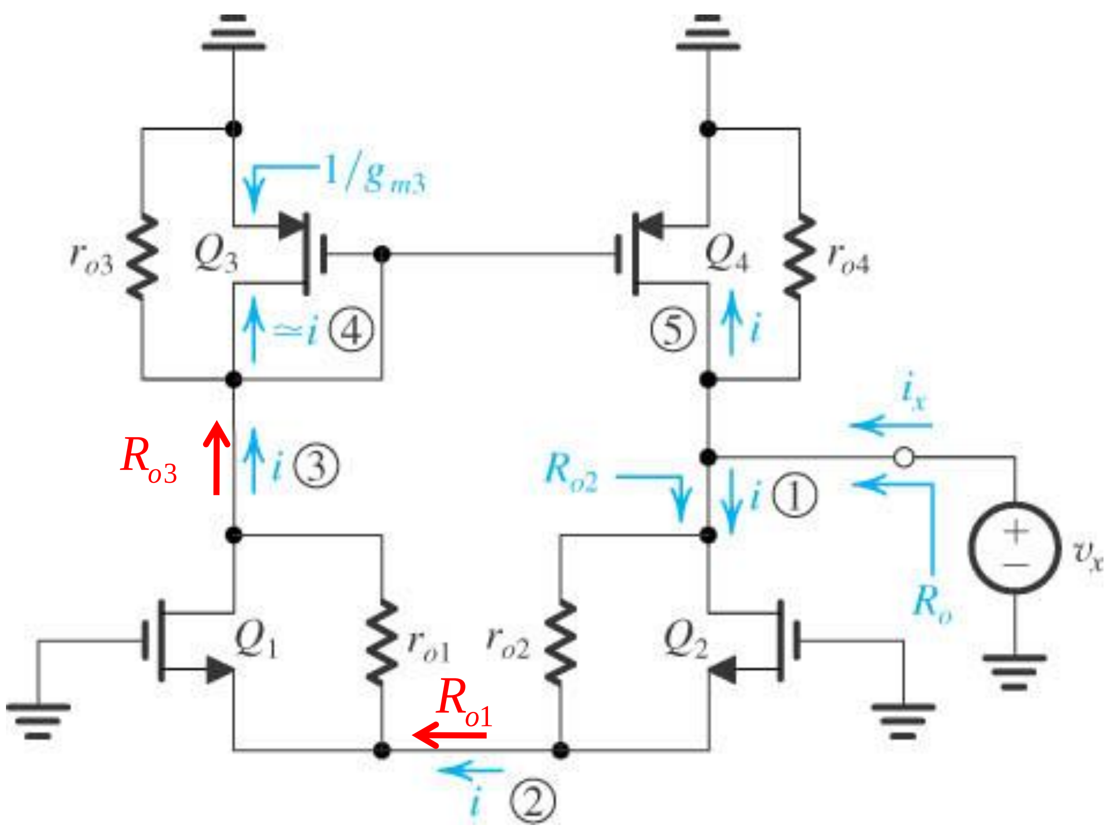
$$\Rightarrow R_{o2} \approx r_{o2} + \left(1 + g_{m2} r_{o2}\right)\frac{1}{g_{m1}}$$

$$\Downarrow \quad g_{m1} = g_{m2}$$

$$\Rightarrow R_{o2} \approx 2 r_{o2}$$

Differential amplifier with active load

Output resistance R_o – step 4: compute R_o



$$i_x = i + i + \frac{v_x}{r_{o4}}$$

$$i = v_x / R_{o2}$$

$$i_x = 2\frac{v_x}{R_{o2}} + \frac{v_x}{r_{o4}}$$

$$\Rightarrow i_x \approx \frac{v_x}{r_{o2}} + \frac{v_x}{r_{o4}}$$

$$\boxed{\Rightarrow R_o = r_{o2} \parallel r_{o4}}$$

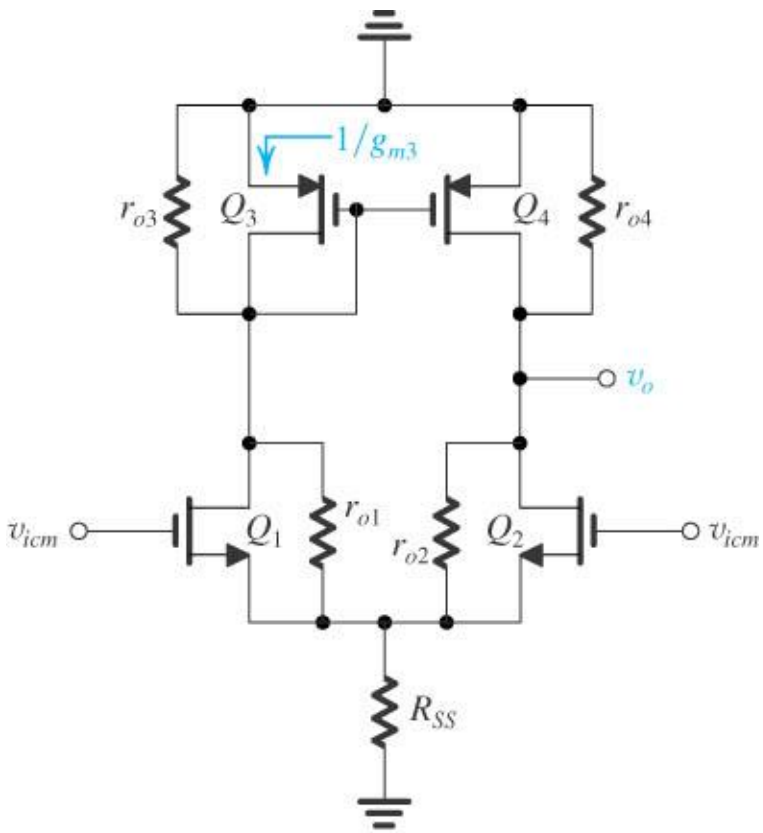
$$\Rightarrow A_d = R_o g_m$$

$$\boxed{\Rightarrow A_d = \left(r_{o2} \parallel r_{o4}\right) g_m}$$

Differential amplifier with active load

Common-mode gain and CMRR

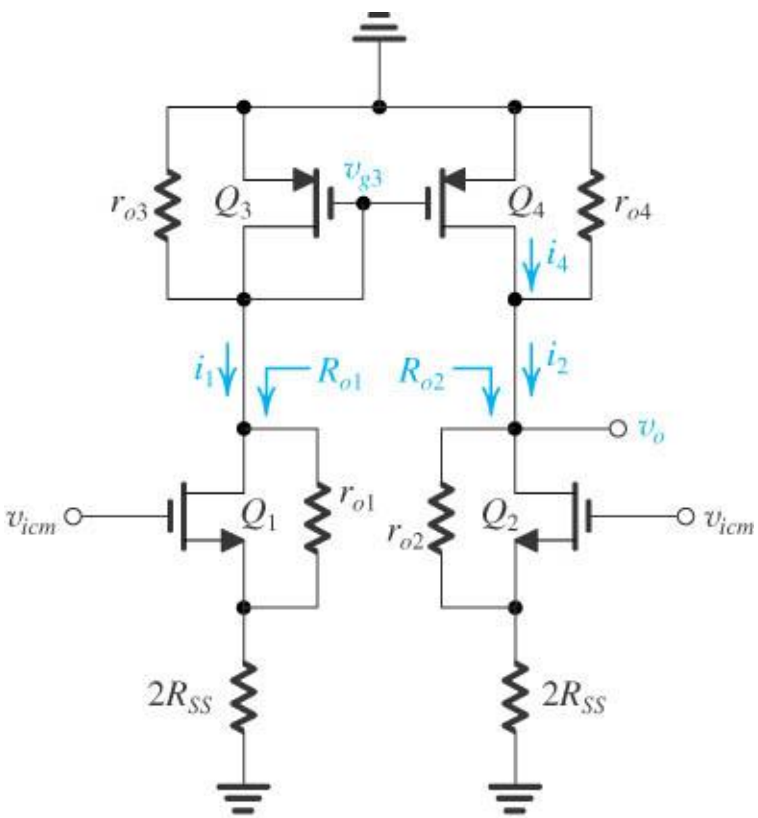
- Effect of current source resistance R_{SS}



Equal current in both branches
$\Rightarrow$Split R_{SS} into $2R_{SS}$ on each branch

Differential amplifier with active load

Common-mode gain and CMRR



R_{SS} large => $i_1 = i_2 \approx \dfrac{v_{icm}}{2R_{SS}}$

$$R_{o1} = R_{o2} = r_o + 2R_{SS} + 2g_m r_o R_{SS}$$

$$v_{g3} = -i_1\left(\frac{1}{g_{m3}} \| r_{o3}\right)$$

$$i_4 = -g_{m4} v_{g3}$$

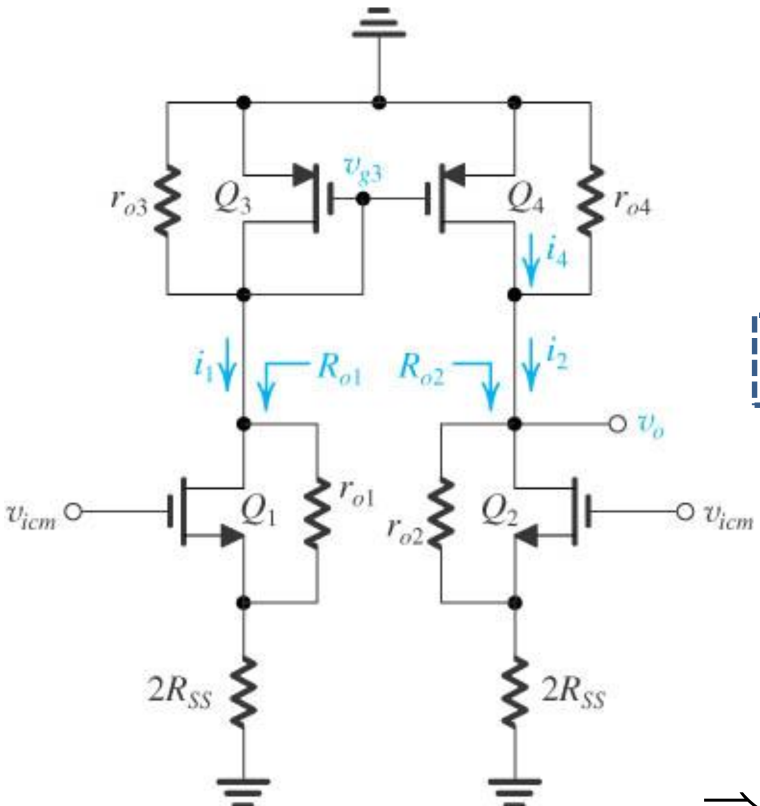
$$= i_1 g_{m4}\left(\frac{1}{g_{m3}} \| r_{o3}\right)$$

$$v_o = r_{o4}\left(i_4 - i_2\right)$$

$$= r_{o4}\left[i_1 g_{m4}\left(\frac{1}{g_{m3}} \| r_{o3}\right) - i_2\right]$$

Differential amplifier with active load

Common-mode gain and CMRR



R_{SS} large => $i_1 = i_2 \approx \dfrac{v_{icm}}{2R_{SS}}$

$$v_o = r_{o4}\left[g_{m4}\left(\frac{1}{g_{m3}} \parallel r_{o3}\right) - 1\right]\frac{v_{icm}}{2R_{SS}}$$

$$\boxed{g_{m3} = g_{m4}}$$

$$\Rightarrow A_{cm} = \frac{v_o}{v_{icm}} = -\frac{1}{2R_{SS}}\frac{r_{o4}}{1+g_{m3}r_{o3}}$$

$$\Rightarrow A_{cm} \approx -\frac{1}{2g_{m3}R_{SS}}$$

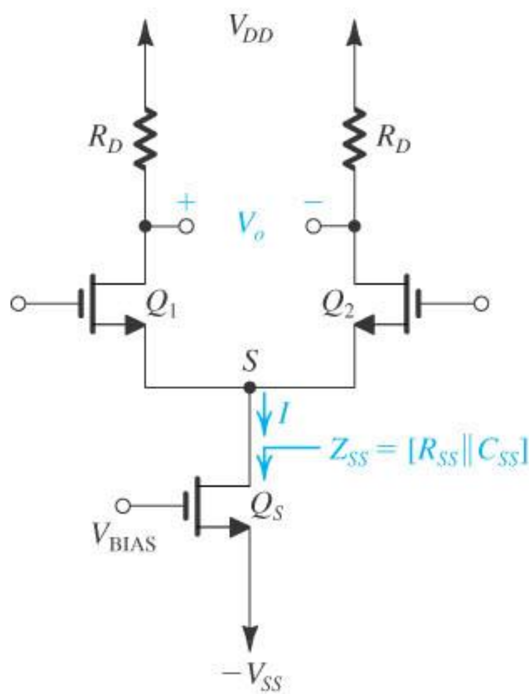
$$\Rightarrow \text{CMRR} = \left|\frac{A_d}{A_{cm}}\right| = \left[g_m\left(r_{o2} \parallel r_{o4}\right)\right]\left[2g_{m3}R_{SS}\right]$$

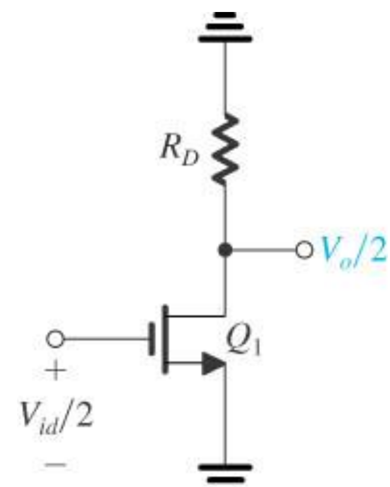
$$\boxed{\text{if } g_{m3} = g_m \text{ and } r_{o2} = r_{o4} = r_o} \quad \Rightarrow \text{CMRR} = \left(g_m r_o\right)\left(g_m R_{SS}\right)$$

Frequency response of differential amplifier

Resistively-loaded MOS amplifier

- Capacitance C_{SS} contains:
  - C_{db} and C_{gd} of Q_S
  - C_{sb} of Q_1 and C_{sb} of Q_2
- No change for differential input



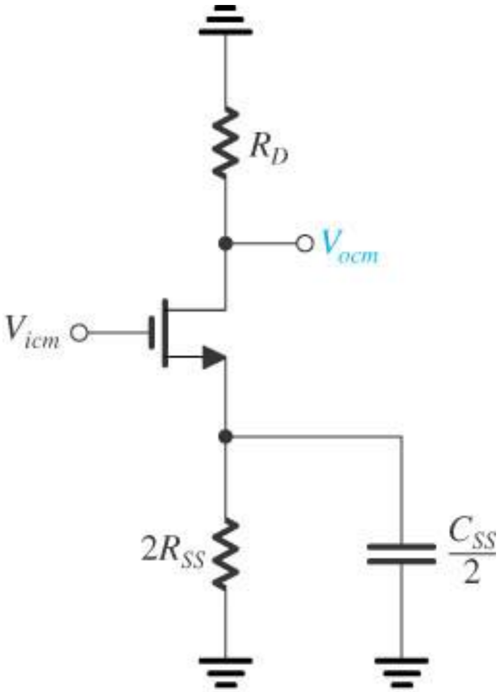


Frequency response of differential amplifier

Resistively-loaded MOS amplifier

- Common-mode half-circuit:
  - Frequency of $C_{SS}/2$ and $2R_{SS}$ is much lower than frequency de to other capacitances

=> Other capacitances (C_{gs}, C_{gd}, C_{db}) of transistors ignored



Reminder: $A_{cm} = -\dfrac{\Delta R_D}{2R_{SS}}$

$$\Rightarrow A_{cm} = -\frac{\Delta R_D}{2Z_{SS}} = -\frac{\Delta R_D}{2} Y_{SS}$$

$$\Rightarrow A_{cm} = -\frac{\Delta R_D}{2}\left(\frac{1}{R_{SS}} + j\omega C_{SS}\right)$$

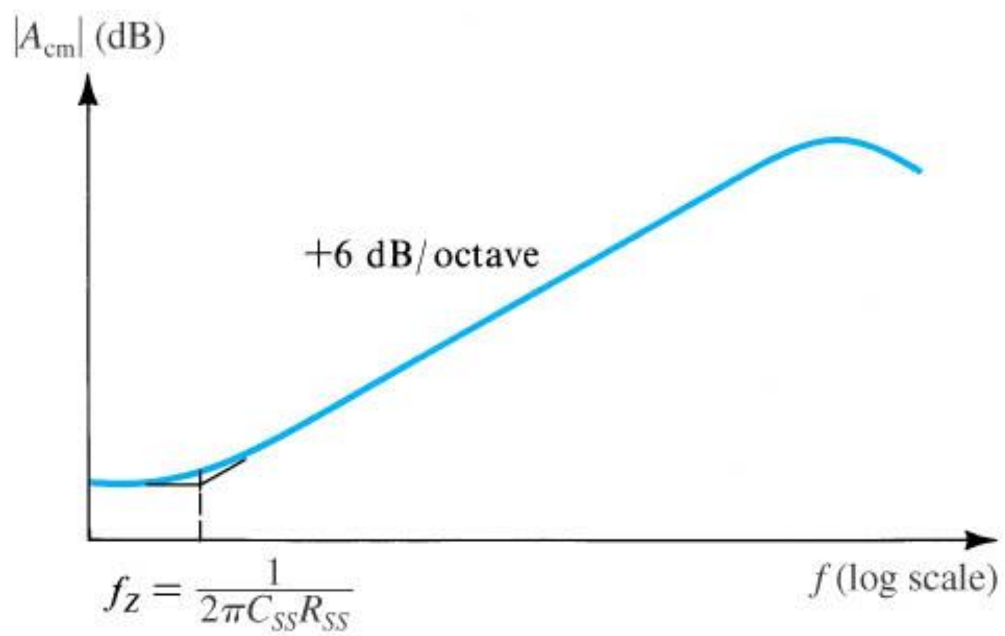
$$\boxed{\Rightarrow A_{cm} = -\frac{\Delta R_D}{2R_{SS}}\left(1 + j\omega R_{SS} C_{SS}\right)}$$

$$\boxed{\Rightarrow f_Z = \frac{1}{2\pi R_{SS} C_{SS}}}$$

Frequency response of differential amplifier

Resistively-loaded MOS amplifier

- A_{cm} increases with frequency
  - $\Rightarrow$ At some point, other capacitances of transistor kick in
  - $\Rightarrow$ A_{cm} starts to decrease



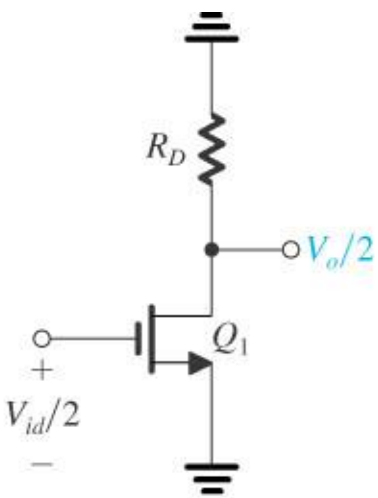
Frequency response of differential amplifier

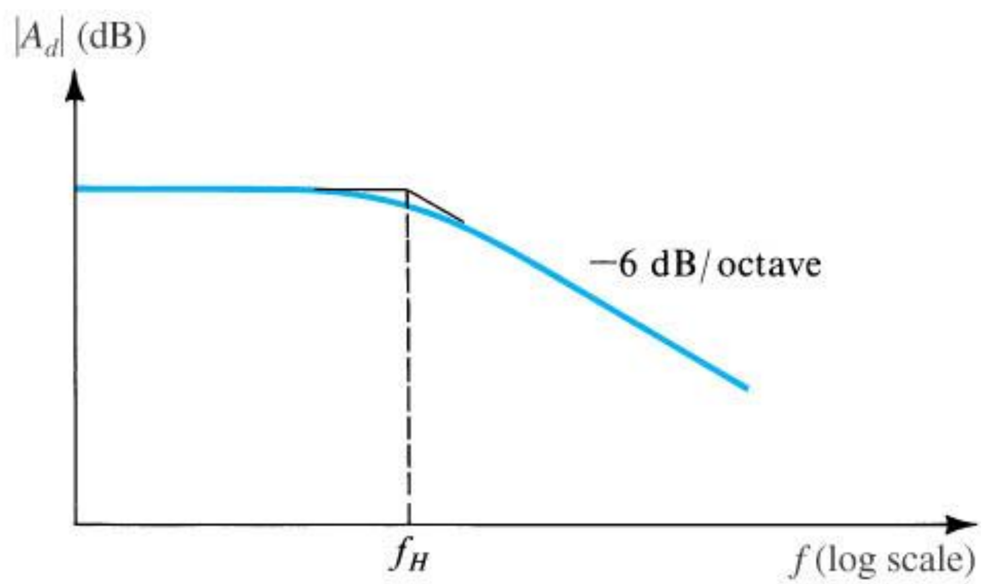
Resistively-loaded MOS amplifier

- Differential signal

  $\Rightarrow$ common-source amplifier

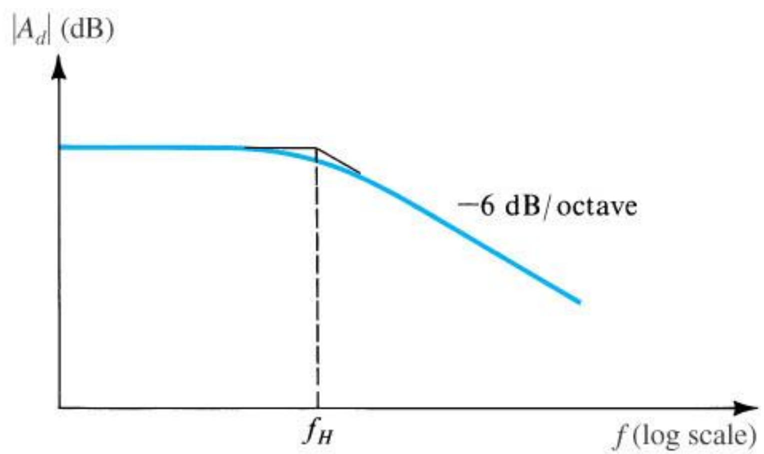
  $\Rightarrow$ See frequency response of CS amplifier in previous chapter

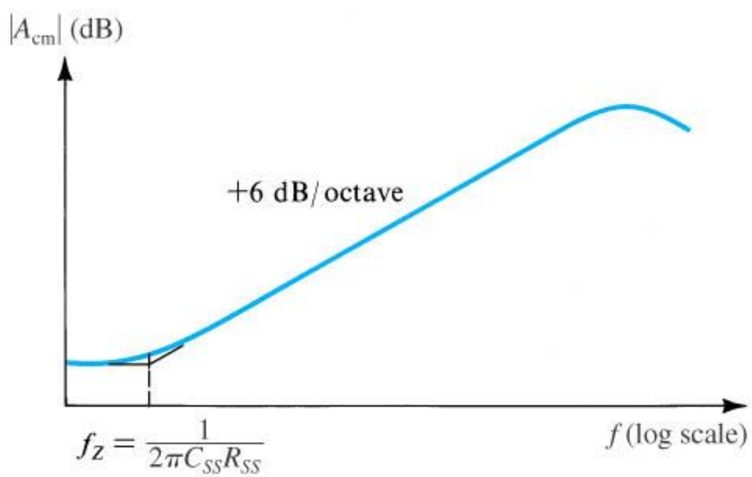


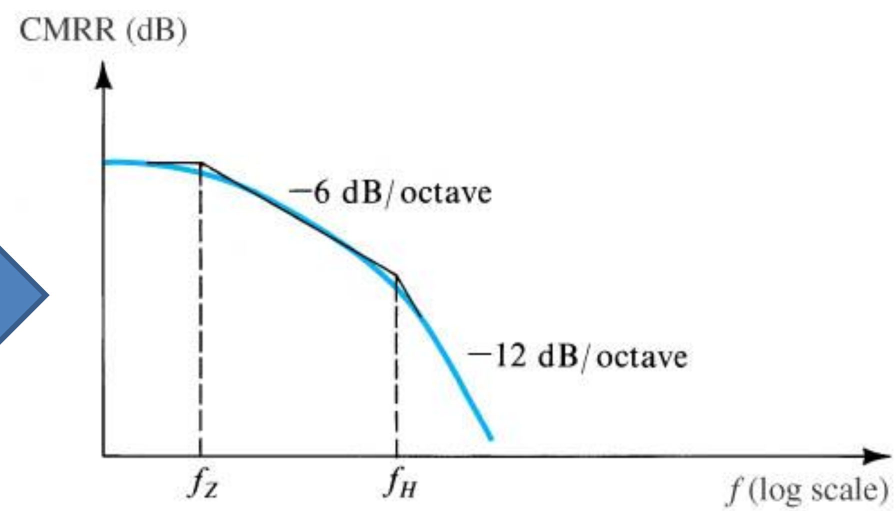


Frequency response of differential amplifier

Resistively-loaded MOS amplifier







$\Rightarrow$ CMRR decreases (strongly) with frequency, starting at f_Z

Frequency response of differential amplifier

Active-loaded MOS amplifier

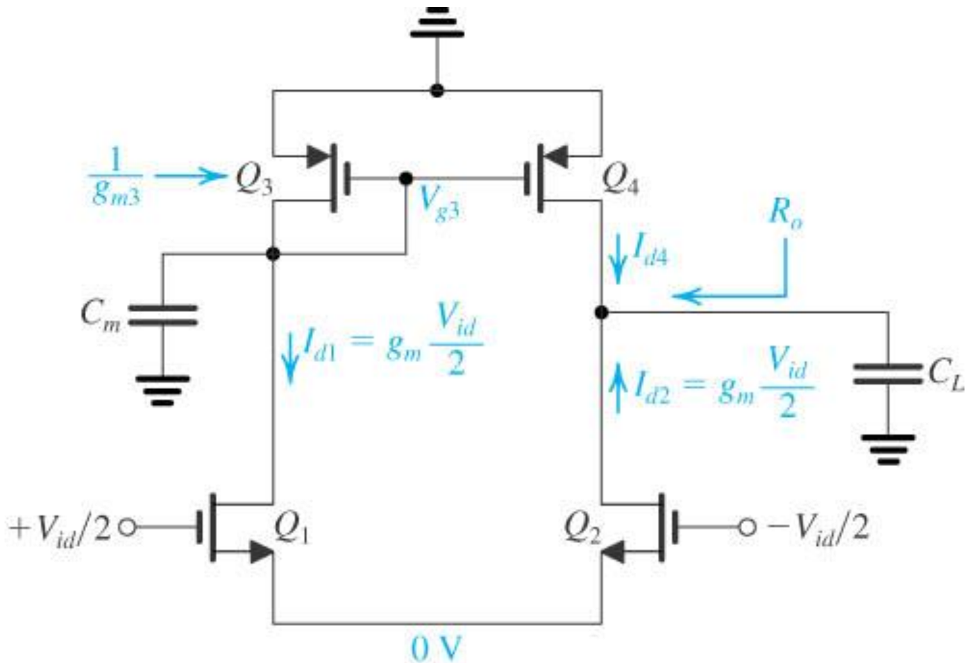
- Capacitance C_m formed by several capacitances:

$$C_m = C_{gd1} + C_{db1} + C_{db3} + C_{gs3} + C_{gs4}$$

- Capacitance C_L formed by several capacitances:

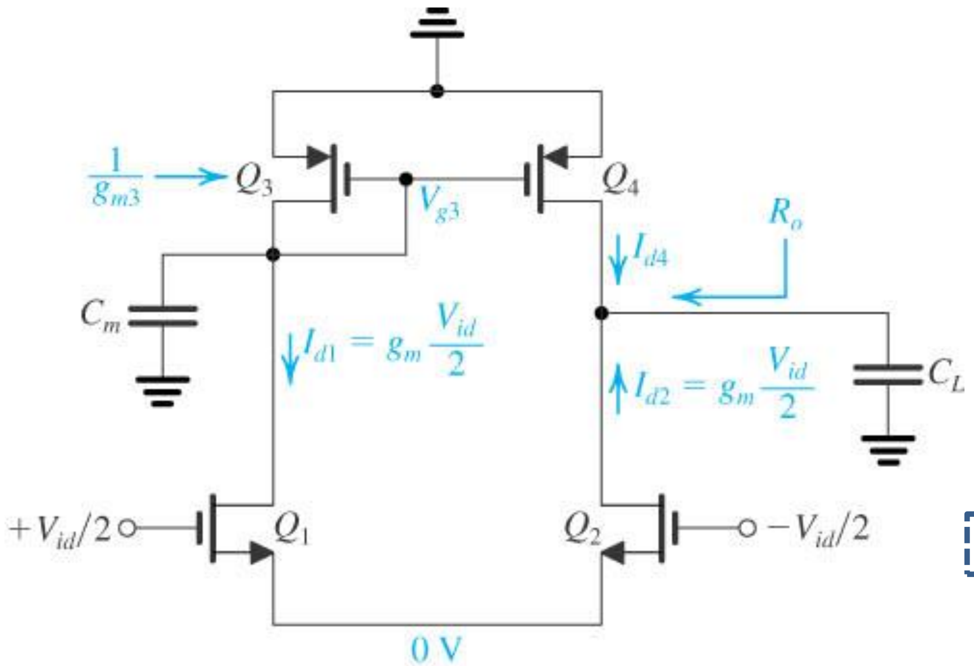
$$C_L = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_x$$

Load capacitance



Frequency response of differential amplifier

Active-loaded MOS amplifier



$$I_{d1} = g_m V_{id} / 2$$

$$V_{g3} = \left(\frac{1}{g_{m3}} \parallel C_m \right) I_{d1}$$

$$\Rightarrow V_{g3} = -\frac{g_m}{g_{m3} + j\omega C_m} \frac{V_{id}}{2}$$

$$I_{d4} = -g_{m4} V_{g3}$$

$$\boxed{g_{m3} = g_{m4}}$$

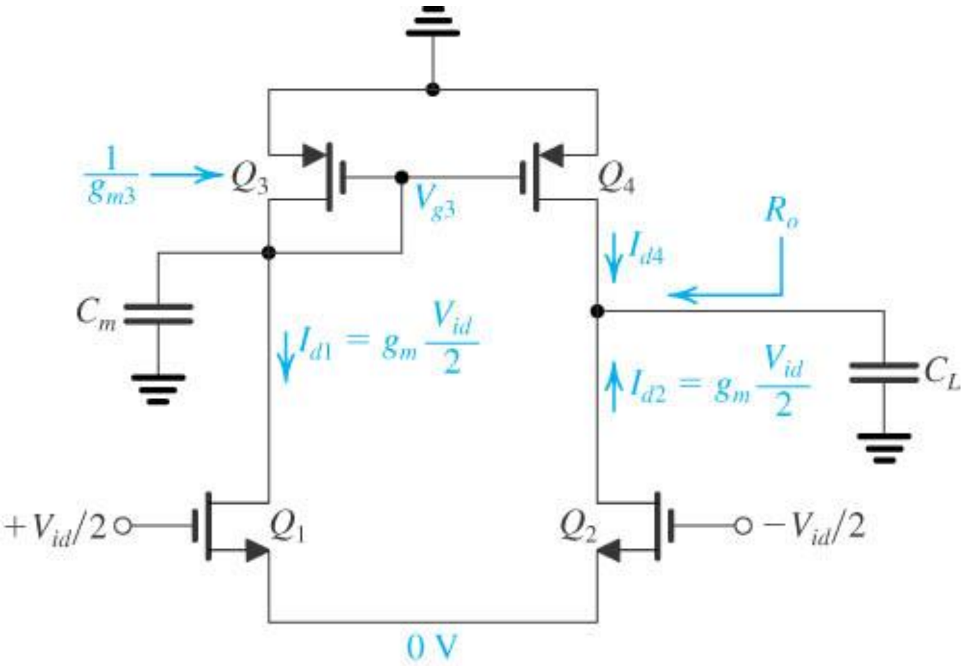
$$\Rightarrow I_{d4} = \frac{g_m V_{id} / 2}{1 + j\omega C_m / g_{m3}}$$

$$I_o = I_{d4} + I_{d2}$$

$$\Rightarrow I_o = \frac{g_m V_{id} / 2}{1 + j\omega C_m / g_{m3}} + g_m \left(V_{id} / 2 \right)$$

Frequency response of differential amplifier

Active-loaded MOS amplifier



$$I_o = \frac{g_m V_{id}/2}{1 + j\omega C_m / g_{m3}} + g_m \left(V_{id}/2 \right)$$

$$V_o = I_o \left(R_o \parallel C_L \right)$$

$$\Rightarrow V_o = g_m R_o \left(\frac{V_{id}}{2} \right) \left[1 + \frac{1}{1 + \frac{j\omega C_m}{g_{m3}}} \right] \frac{1}{1 + j\omega C_L R_o}$$

Frequency response of differential amplifier

Active-loaded MOS amplifier

$$V_o = g_m R_o \left(\frac{V_{id}}{2}\right)\left[1+\frac{1}{1+\frac{j\omega C_m}{g_{m3}}}\right]\frac{1}{1+j\omega C_L R_o} \Rightarrow A_d = (g_m R_o)\left(\frac{1}{1+j\omega C_L R_o}\right)\left(\frac{1+\frac{j\omega C_m}{2g_{m3}}}{1+\frac{j\omega C_m}{g_{m3}}}\right)$$

$$\Rightarrow f_{P1} = \frac{1}{2\pi C_L R_o}$$

Often dominant pole

$$\Rightarrow f_{P2} = \frac{g_{m3}}{2\pi C_m}$$

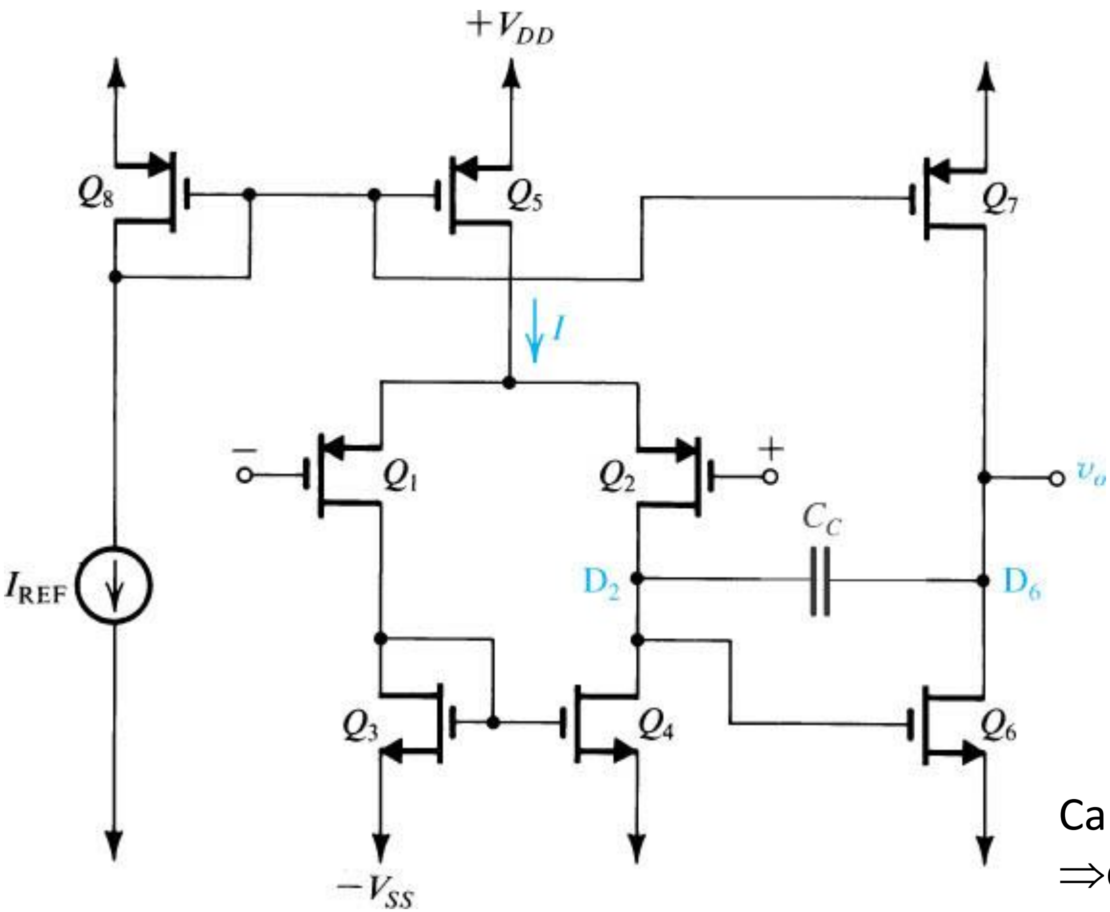
$$\Rightarrow f_Z = \frac{2g_{m3}}{2\pi C_m}$$

Very high frequency!

Note that f_Z due to current source is usually main cause of CMRR degradation

Multistage amplifier

Two-stage CMOS amplifier



- Q1-Q2 MOS differential amplifier with active load (Q3-Q4)
- Q6 common-source amplifier
- Current mirror Q8-Q5 for polarizing Q1-Q2
- Current mirror Q8-Q7 for polarising Q6

$$A_1 = -g_{m1}\left(r_{o2} \parallel r_{o4}\right)$$

$$A_2 = -g_{m6}\left(r_{o6} \parallel r_{o7}\right)$$

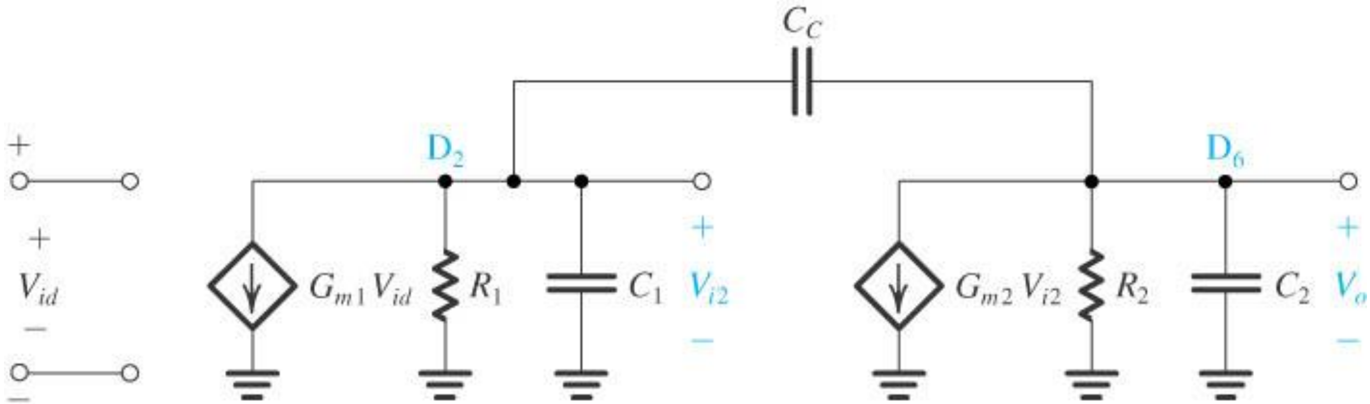
$$\Rightarrow A_{tot} = A_1 A_2$$

$$R_o = \left(r_{o6} \parallel r_{o7}\right)$$

Capacitor C_c (see next slide)
⇒dominant pole
⇒-20dB/decade
⇒stability

Multistage amplifier

Frequency response



$$C_1 = C_{gd4} + C_{db4} + C_{gd2} + C_{db2} + C_{gs6}$$

$$C_2 = C_{db6} + C_{db7} + C_{gd7} + C_L$$

$$\Rightarrow f_Z = \frac{G_{m2}}{2\pi C_C}$$

$$\Rightarrow f_{P1} \approx \frac{1}{2\pi R_1\left[C_1 + C_C\left(1+G_{m2}R_2\right)\right]}$$

$$\Rightarrow f_{P2} \approx \frac{G_{m2}}{C_2}$$

Choose C_C so that f_{P1} lower than f_Z and f_{P2}, in order to ensure -20dB/decade