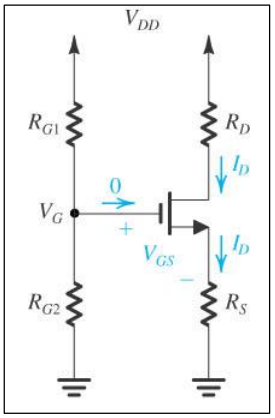
Chapter 4 : Single-stage MOS amplifiers - exercices

BIASING IN MOS AMPLIFIER CIRCUITS

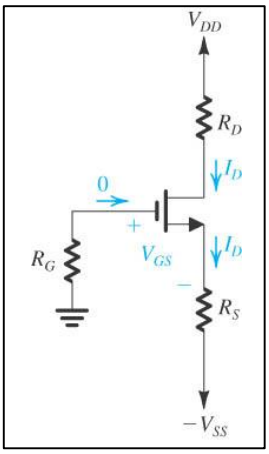
Exercise 1 (D4.55)



Consider the classical biasing circuit shown in the figure, using a 15-V supply. For the NMOS, $V_t = 1.2\,V$, $\lambda = 0$, $\frac{k'_n W}{L} = 3200\,\mu A/V^2$. Arrange that the drain current is $2\,mA$, with one-third of the supply voltage across each of R_S and R_D. Use $22\,M\Omega$ for the larger of R_{G1} and R_{G2}.

a) What are the values of R_{G1}, R_{G2}, R_S and R_D?
b) How far is the drain voltage from the edge of saturation?

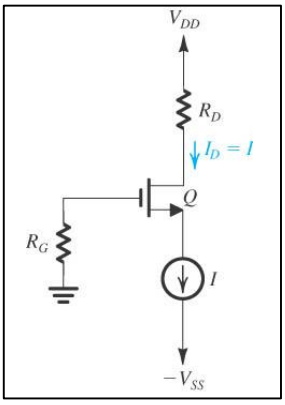
Exercise 2 (D4.56)



Using the circuit topology displayed in the figure, arrange to bias the NMOS transistor at $I_D = 2\,mA$ with V_D midway between cutoff and the beginning of the triode operation. The available supplies are $\pm 15\,V$. For the NMOS transistor, $V_t = 0.8\,V$, $\lambda = 0$, $\frac{k'_n W}{L} = 2500\,\mu A/V^2$. Use a gate-bias resistor of $10\,M\Omega$.

a) What are the values of R_S and R_D?

Exercise 3 (D4.63)

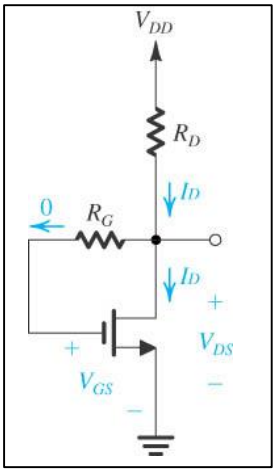


For the circuit shown in the figure, with $I = 1\,mA$, $R_G = 0\,\Omega$, $R_D = 5\,k\Omega$ and $V_{DD} = 10\,V$, the NMOS transistor has the following characteristics: $V_t = 1\,V$, $\lambda = 0$, $\frac{k'_n W}{L} = 0.5\,mA/V^2$.

a) What are the values of V_S, V_D and V_{DS}?

Exercise 4 (D4.64)

In the circuit of the figure, let $R_G = 10\ M\Omega$, $R_D = 10\ k\Omega$ and $V_{DD} = 10\ V$. The NMOS transistor has $V_t = 1\ V, \lambda = 0, \frac{k_n' W}{L} = 0.5\ mA/V^2$.



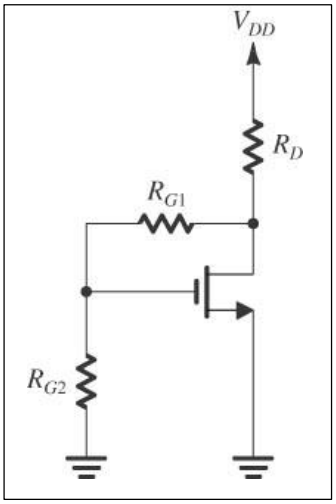
a) What are the values of V_D and V_G?

Exercise 5 (D4.65)

Using the feedback bias arrangement shown in the figure of exercise 4, with a $9\ V$ supply and an NMOS device for which $V_t = 1\ V, \lambda = 0, \frac{k_n' W}{L} = 0.4\ mA/V^2$, find R_D to establish a drain current of $2\ mA$.

Exercice 6 (D4.66)

The figure shows a variation of the feedback-bias circuit of the previous exercises. Using a $6\ V$ supply with an NMOS transistor for which $V_t = 1.2\ V$, $\lambda = 0$, $\frac{k_n' W}{L} = 3.2\ mA/V^2$, provide a design which biases the transistor at $I_D = 2\ mA$, with V_{DS} large enough to allow saturation operation for a 2-V negative signal swing at the drain. Use $22\ M\Omega$ as the largest resistor in the feedback-bias network.



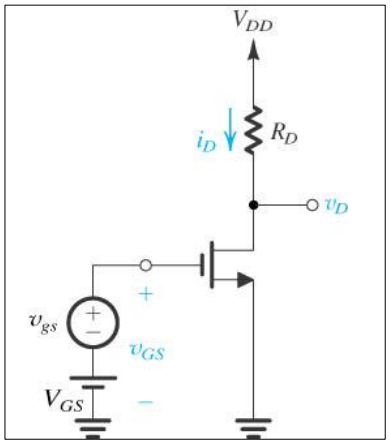
a) What are the values of R_{G1}, R_{G2} and R_D?

SMALL-SIGNAL OPERATION AND MODELS & SINGLE-STAGE MOS AMPLIFIERS

Exercise 7 (D4.69)

Consider te NMOS amplifier of the figure for $V_t = 2\,V$, $\frac{k_n' W}{L} = 1\,mA/V^2$, $V_{GS} = 4\,V$, $V_{DD} = 10\,V$ and $R_D = 3.6\,k\Omega$.

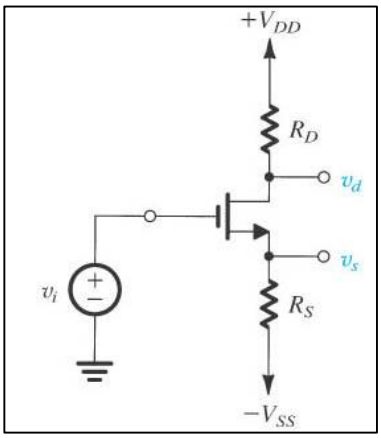
a) Find the DC quantities I_D and V_D
b) Calculate the value of g_m at the bias point
c) Calculate the value of the voltage gain
d) If the NMOS has $\lambda = 0.01\,V^{-1}$, find r_0 at the bias point and calculate the voltage gain.



Exercise 8 (D4.74)

For the NMOS amplifier in the figure, replace the transistor with its T-equivalent circuit. Derive expressions for the voltage gains

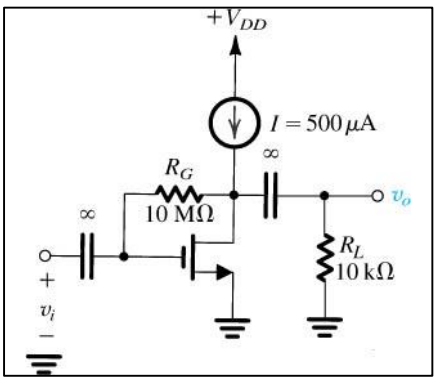
a) v_s/v_i
b) v_d/v_i



Exercise 9 (D4.75)

In the circuit of the figure, the NMOS transistor has $V_t = 0.9\,V$ and $V_A = 50\,V$ and operates with $V_D = 2\,V$.

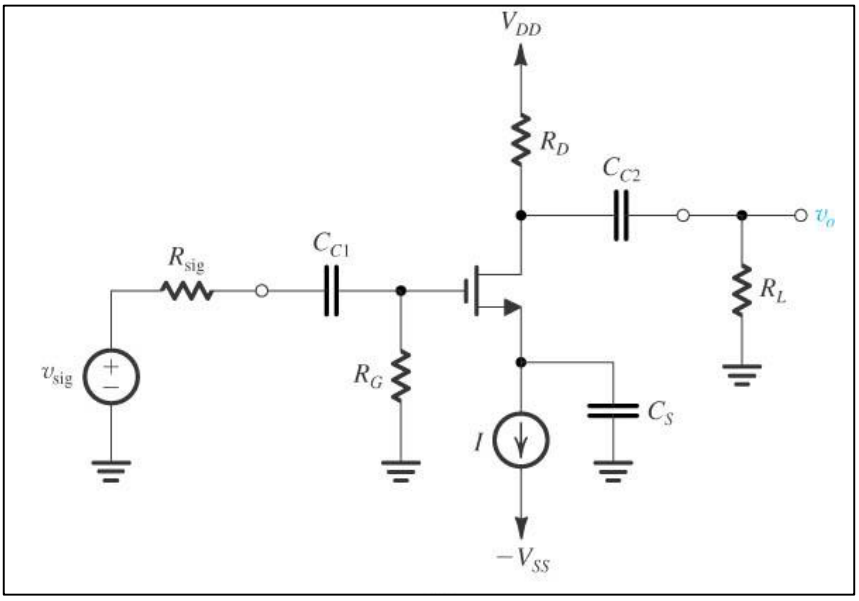
a) What is the voltage gain v_o/v_i ?
b) What do V_D and the gain become if I is increased to $1\,mA$?



Exercise 10 (D4.77)

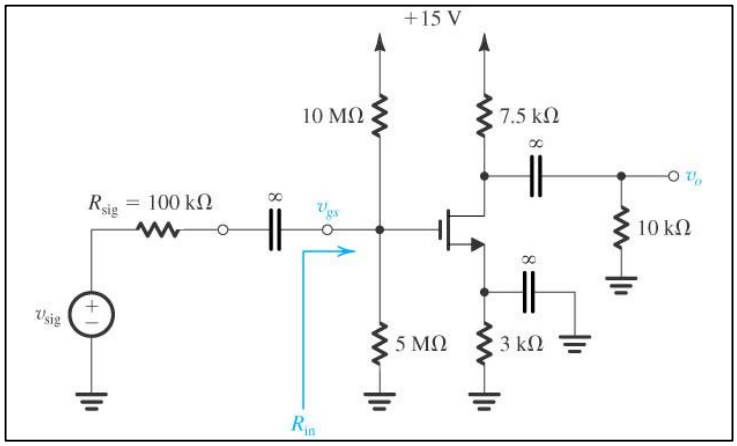
The figure shows a discrete-circuit CS amplifier employing the classical biasing circuit we saw in the lecture. The input signal v_{sig} is coupled to the gate through a very large capacitor (shown as infinite). The transistor source is connected to the ground at signal frequencies via a very large capacitor (shown as infinite). The output voltage that develops at the drain is coupled to a load resistance via a very large capacitor (shown as infinite).

a) If the transistor has $V_t = 1\ V$, and $\frac{k'_n W}{L} = 2\ mA/V^2$, verify that the biasing circuit establishes $V_{GS} = 2\ V$, $I_D = 1\ mA$, and $V_D = +7.5\ V$. That is, assume these values and verify that they are consistent with the values of the circuit components and the device parameters.
b) Find g_m and r_0 if $V_A = 100\ V$
c) Draw a complete small-signal equivalent circuit for the amplifier assuming all capacitors behave as short-circuits at signal frequencies
d) Find R_{in}, v_{gs}/v_{sig}, v_o/v_{gs}, and v_o/v_{sig}



Exercise 11 (D4.82)

A CS amplifier using a NMOS transistor biased in the manner of the figure for which $g_m = 2\ mA/V$ is found to have an overall voltage gain $A_v = -16$. What value of resistance R_S inserted at the source terminal of the NMOS leads to reduce the voltage gain by a factor of 4?



Exercise 12 (D4.88)

a) The NMOS transistor in the source-follower circuit of figure (a) has $g_m = 5\ mA/V$ and a large r_0. Find the open-circuit voltage gain and the output resistance.
b) The NMOS transistor in the common-gate amplifier of figure (b) has $g_m = 5\ mA/V$ and a large r_0. Find the input resistance and the voltage gain.
c) If the output of the source-follower in (a) is connected to the input of the common-gate amplifier in (b), use the previous results to obtain the overall voltage gain v_o/v_i