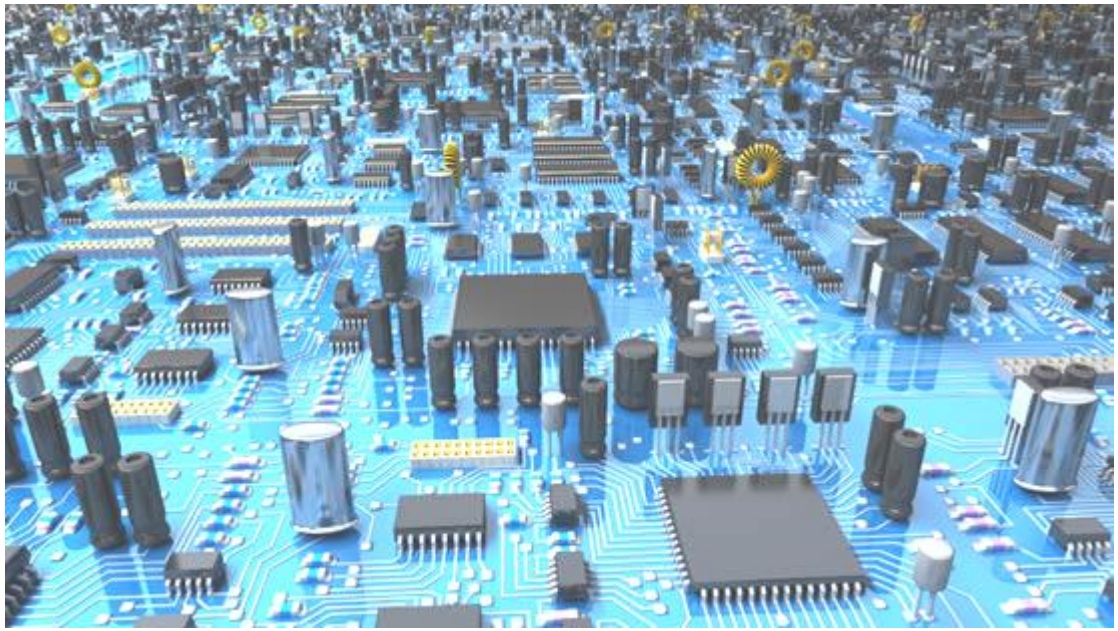
Chapter 3

Metal-Oxyde Semiconductor Field Effect Transistors (MOSFET)



FET: outline

Outline

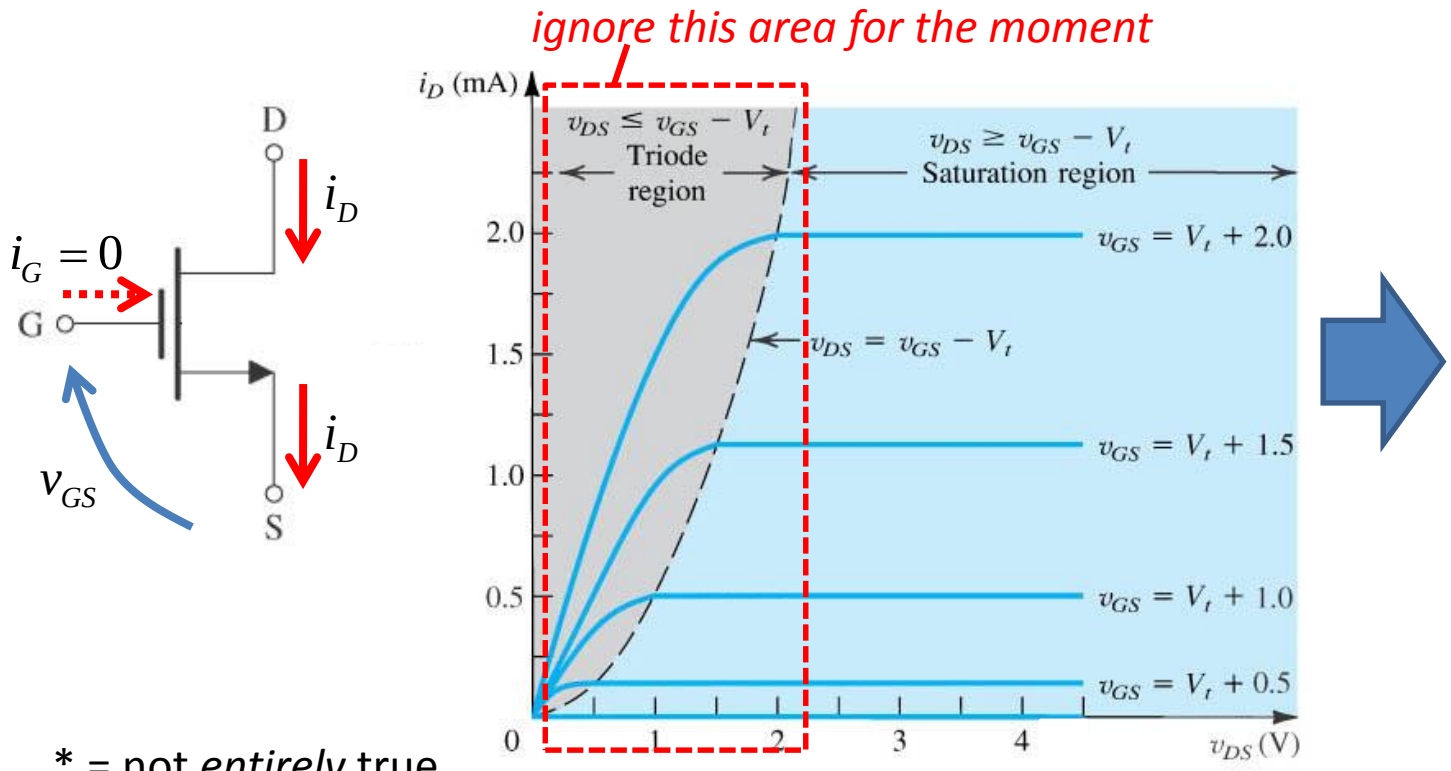
- Enhanced-type MOSFET transistors
  - NMOS: introduction to the I-V characteristics
  - NMOS: Device structure and physical operation
  - NMOS: I-V characteristics (detailled)
  - PMOS and CMOS technology
  - Complements on NMOS technology

- Depletion-type MOSFET
  - Depletion-type NMOS: device structure
  - Depletion-type NMOS: I-V characteristics

MOSFET I-V characteristics

… a bit idealized

- MOSFET is a three-port component *
- Input impedance infinite *
- Current source controlled through input voltage v_{GS} *



1/ Electronic switch

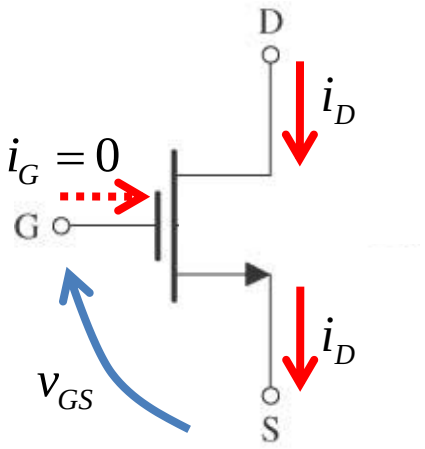
2/ Transcon-ductance amplifier

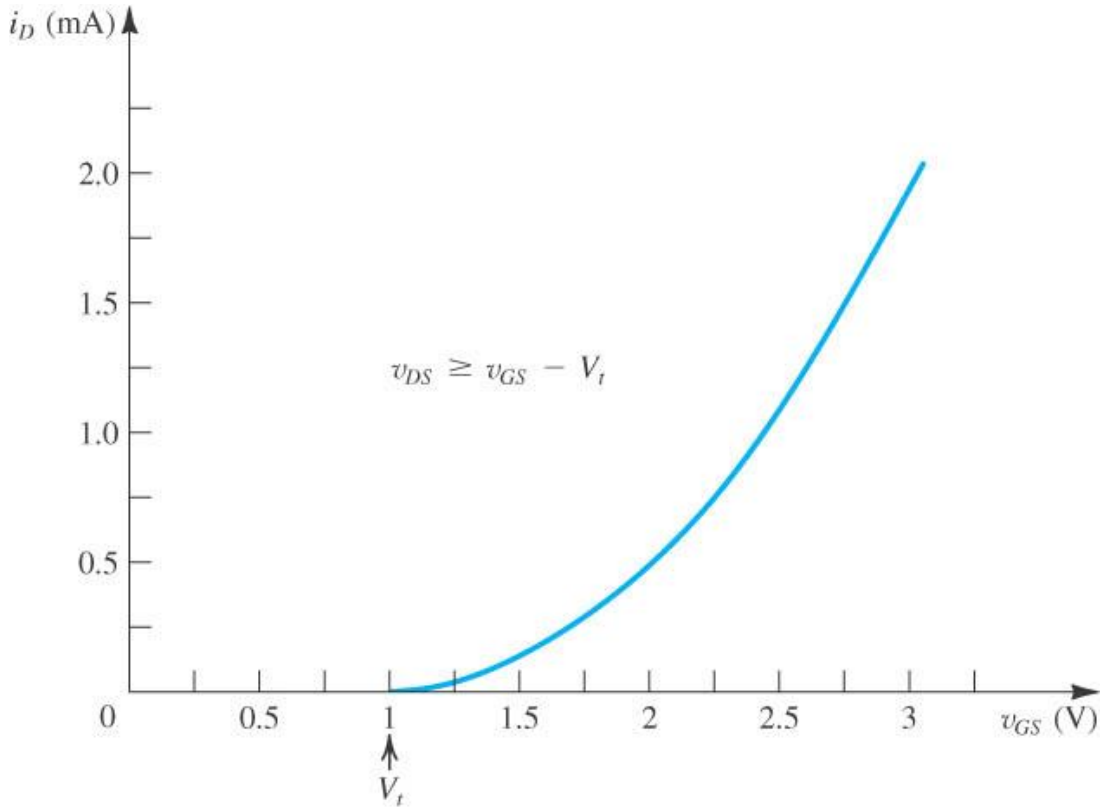
* = not *entirely* true

MOSFET I-V characteristics

… a bit idealized

- Transconductance characteristic
- Magnitude of current source controlled through input voltage



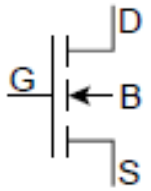


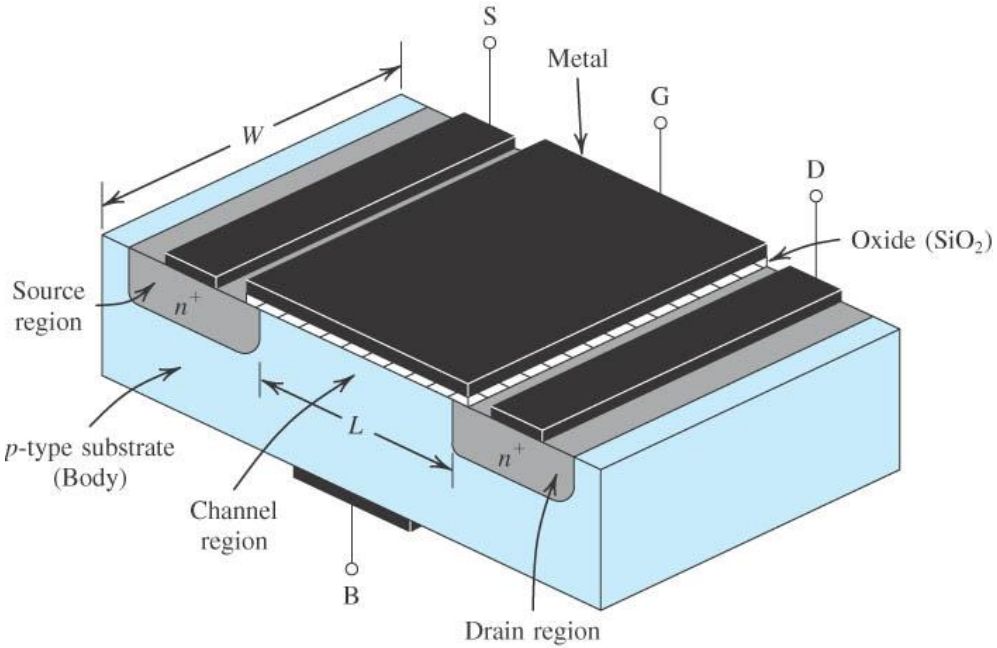
NMOS device structure

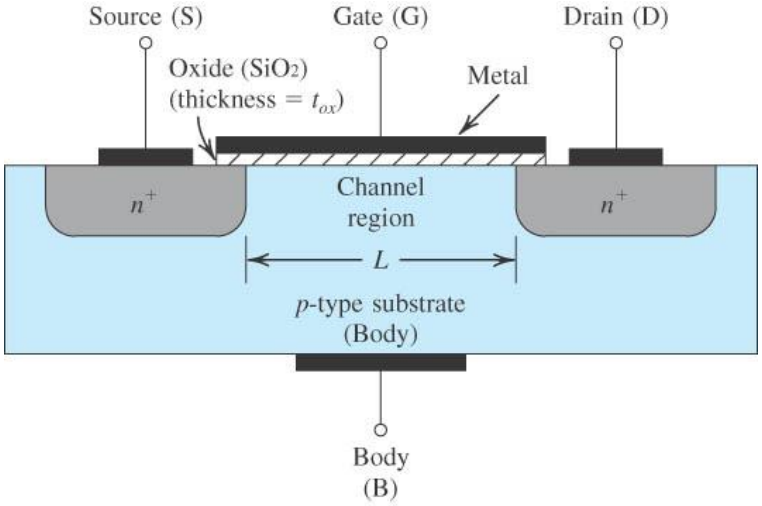
Metal-Oxyde-Semiconductor Field Effect Transistor

- Example of a NPN MOSFET (NMOS transistor)
  - gate electrode is electrically insulated from the body
  - NMOS has 4 terminals (but B often connected to S)
  - n-region heavily doped (n^+)

NMOS symbol:



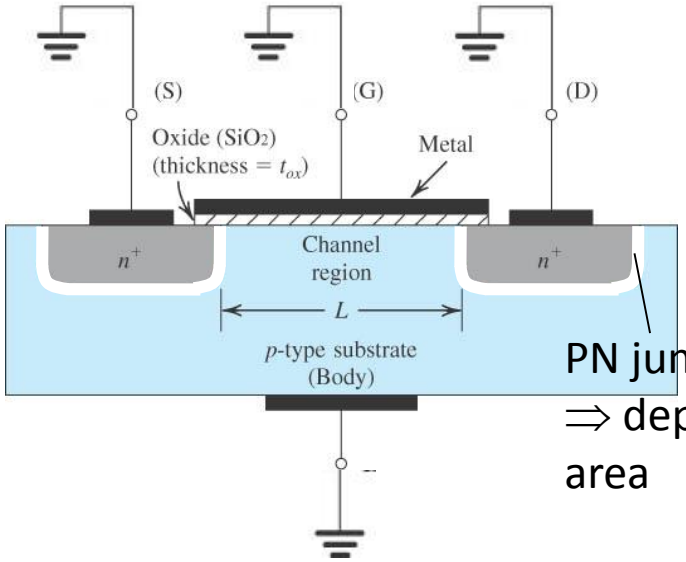




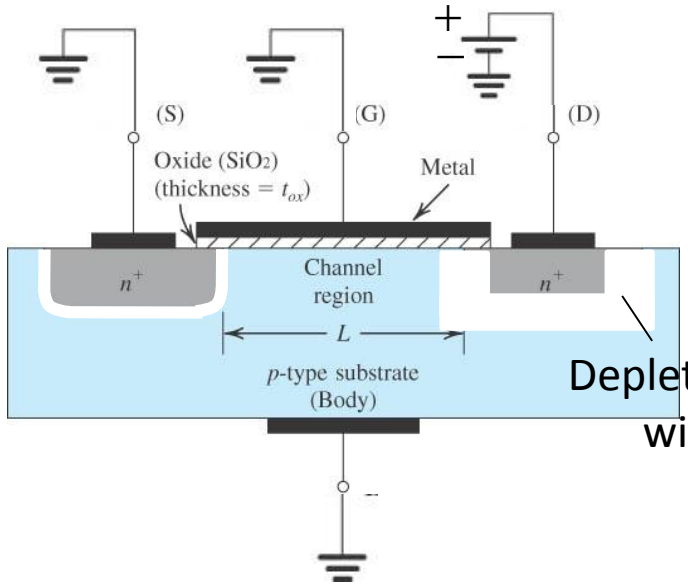
NMOS device structure

No voltage at gate

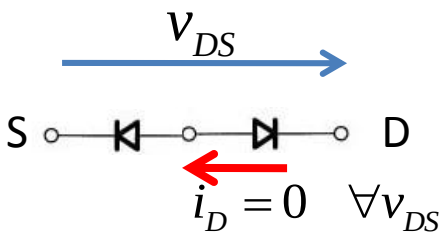
- Equivalent to 2 back-to-back diodes
- No current can flow from drain to source, even for high v_{DS}



PN junction $\Rightarrow$ depletion area



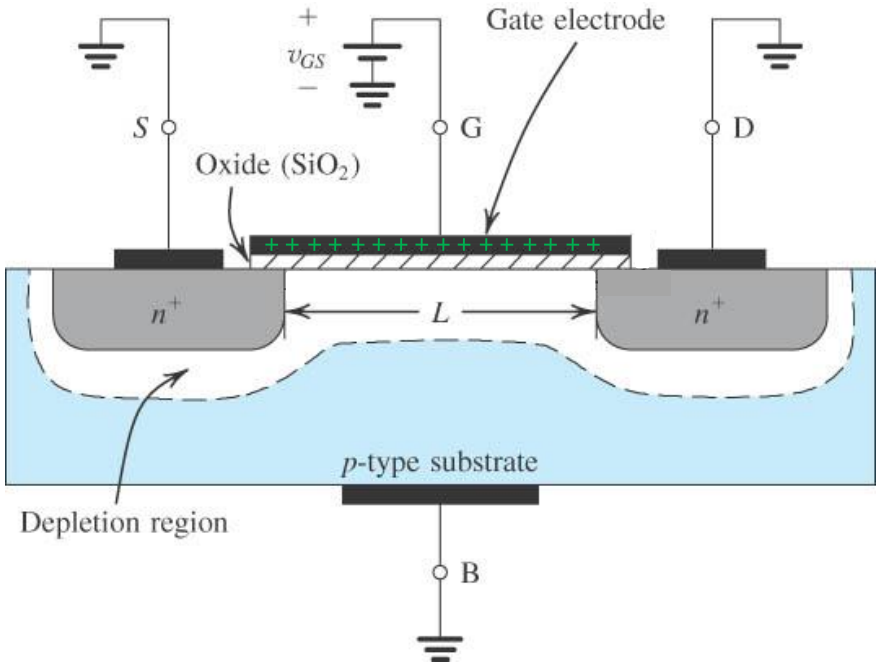
Depletion area widens



NMOS device structure

Increasing voltage at gate

- positive gate voltage repels holes in p-region
  - $\Rightarrow$ creates a depletion region populated by bound negative charges
  - $\Rightarrow$ if $v_{GS} < V_{TH}$, positive charge at gate is compensated for by uncovered bound negative charges



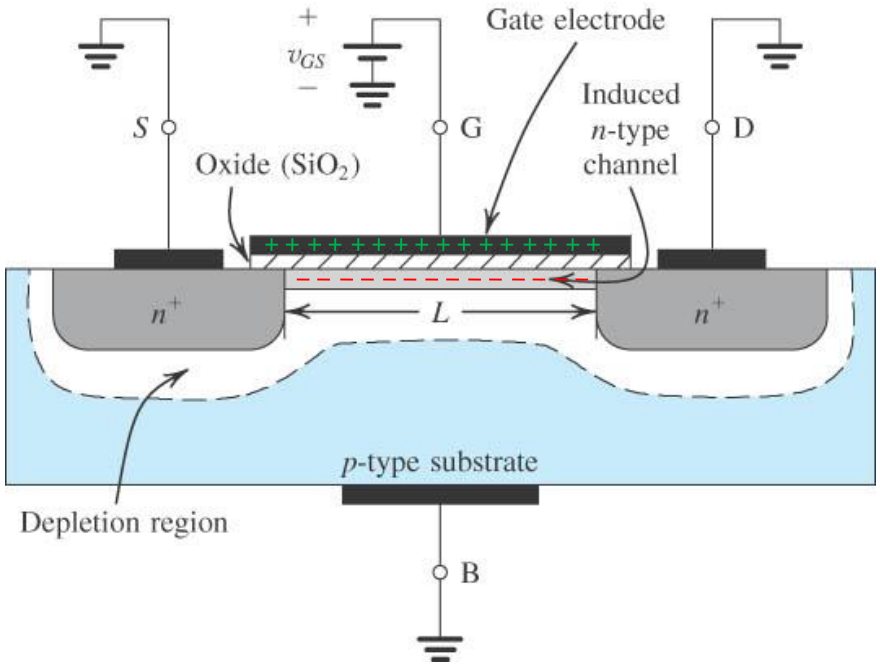
NMOS device structure

Increasing voltage at gate above V_{TH}

$\Rightarrow$ if $v_{GS} \geq V_{TH}$, gate starts attracting electrons from n-regions (as well as minority electrons from p-region)

$\Rightarrow$ n-type channel is created, connecting source and drain

$\Rightarrow$ the higher v_{GS} , the larger the induced channel



NMOS device structure

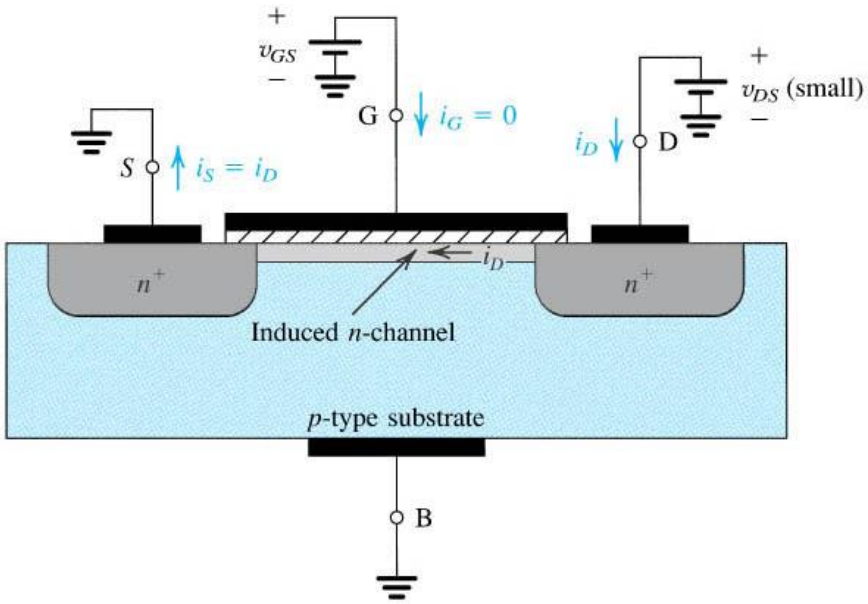
applying a small v_{DS}

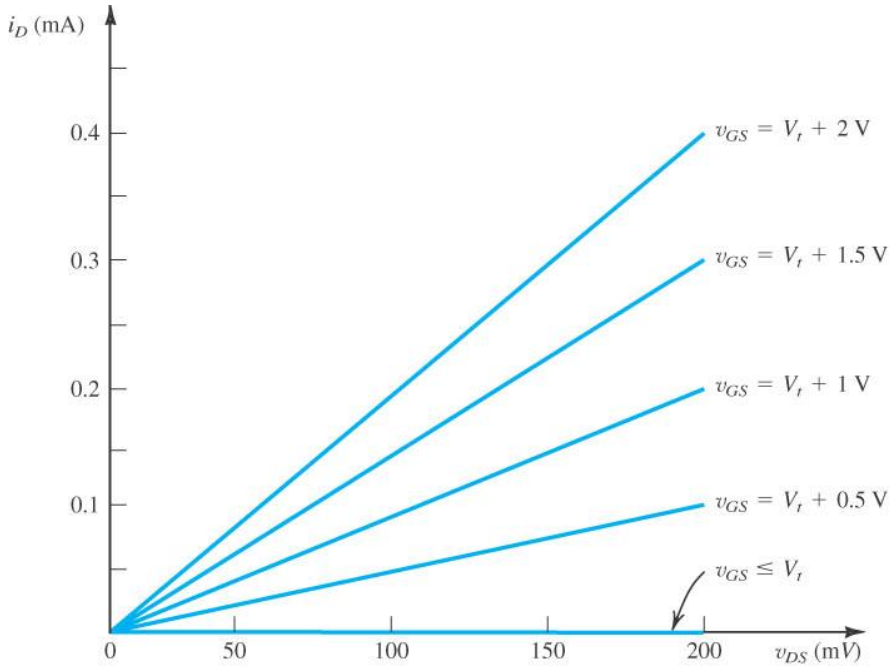
- Electrons start flowing from source to drain

  $\Rightarrow$ current from drain to source

- Increasing v_{GS} widens the channel

  $\Rightarrow$ more currents flows when increasing v_{DS}





NMOS device structure

Higher values of v_{DS}

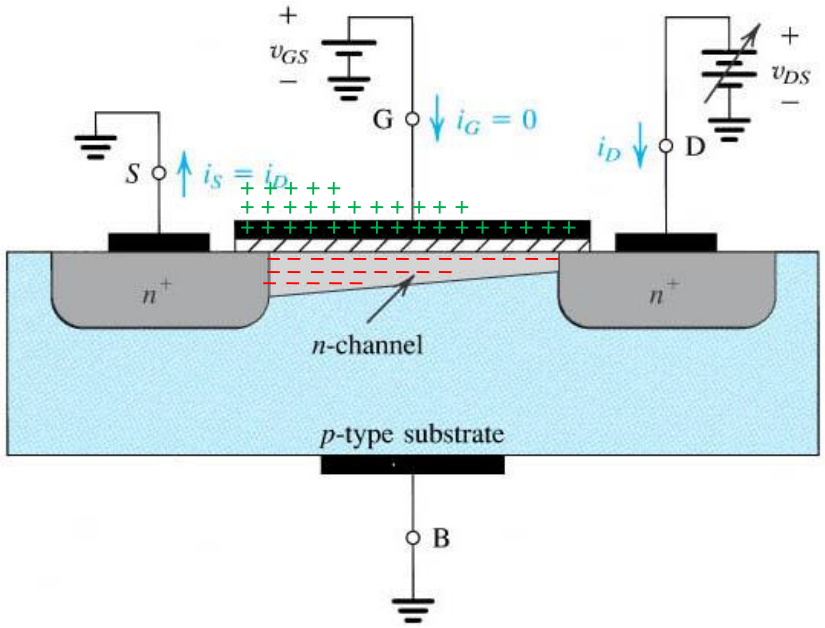
- Gate-substrate voltage is not uniform

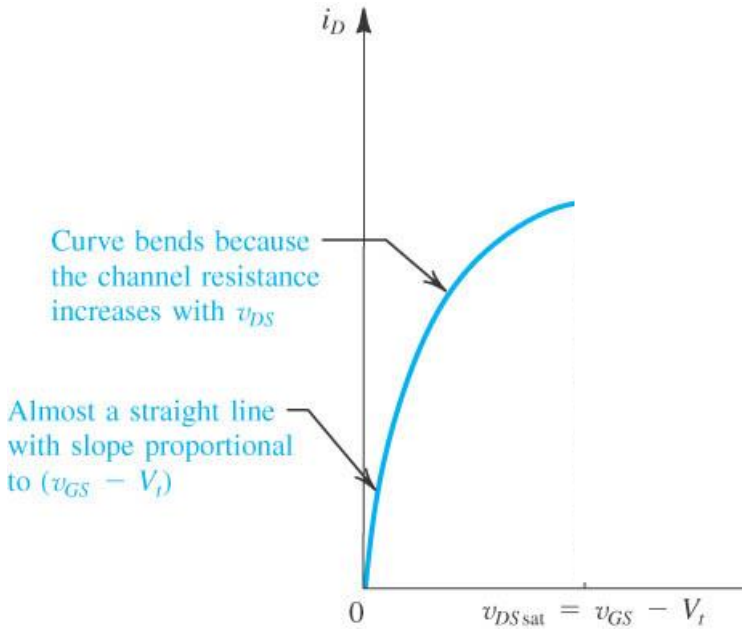
  $\Rightarrow$ Gate-substreate voltage is lower/higher close to drain/source

  $\Rightarrow$ Channel takes tapered form

- Tapered channel => increased resistance

  => i_D-v_{DS} curve bends





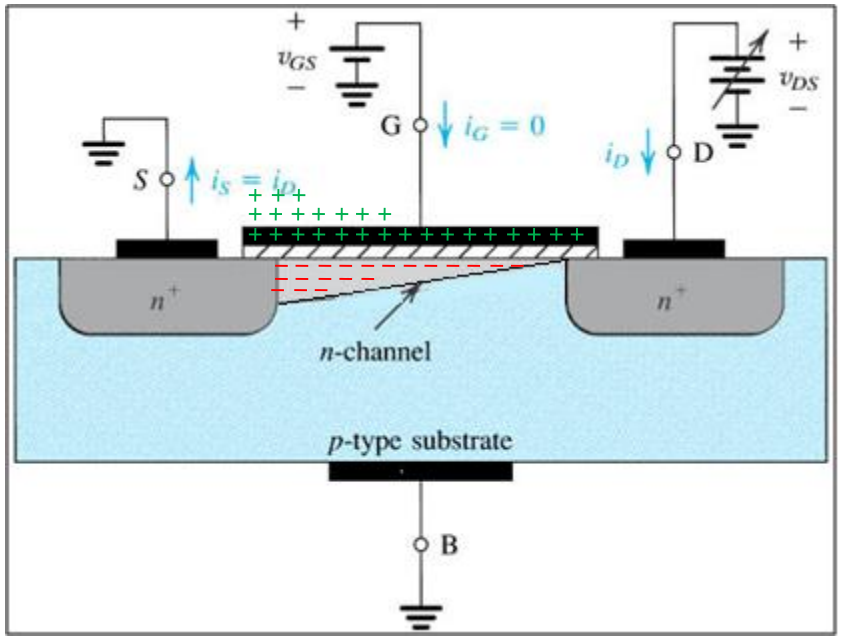
NMOS device structure

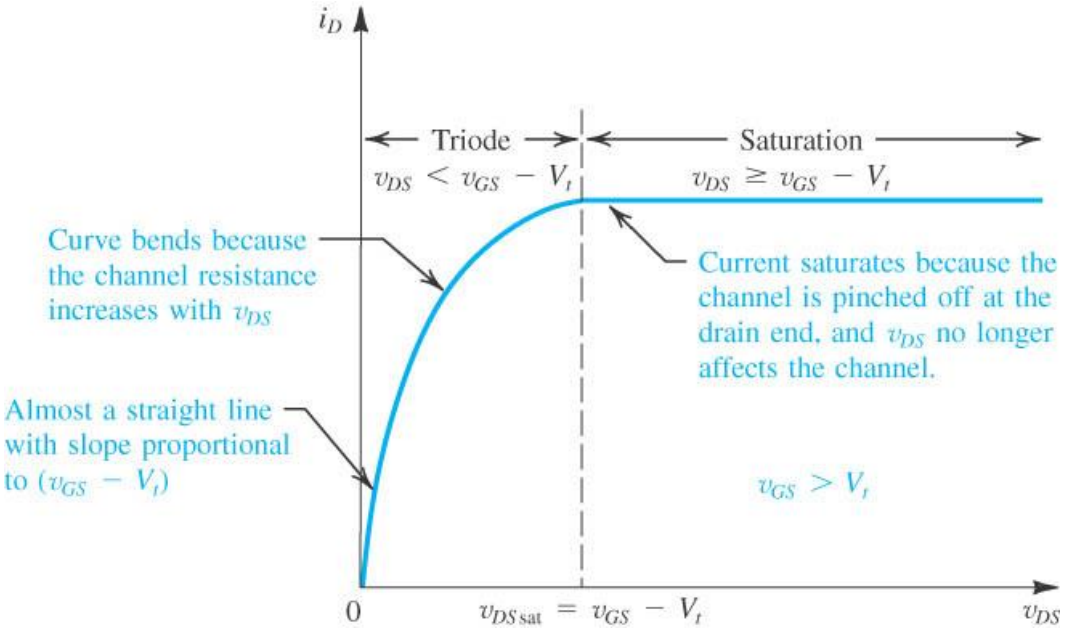
Higher values of v_{DS}

- Eventually, when $v_{DS} \geq v_{GS} - V_T$, channel is pinched off

  $\Rightarrow$ Increase in v_{DS} no longer increases current

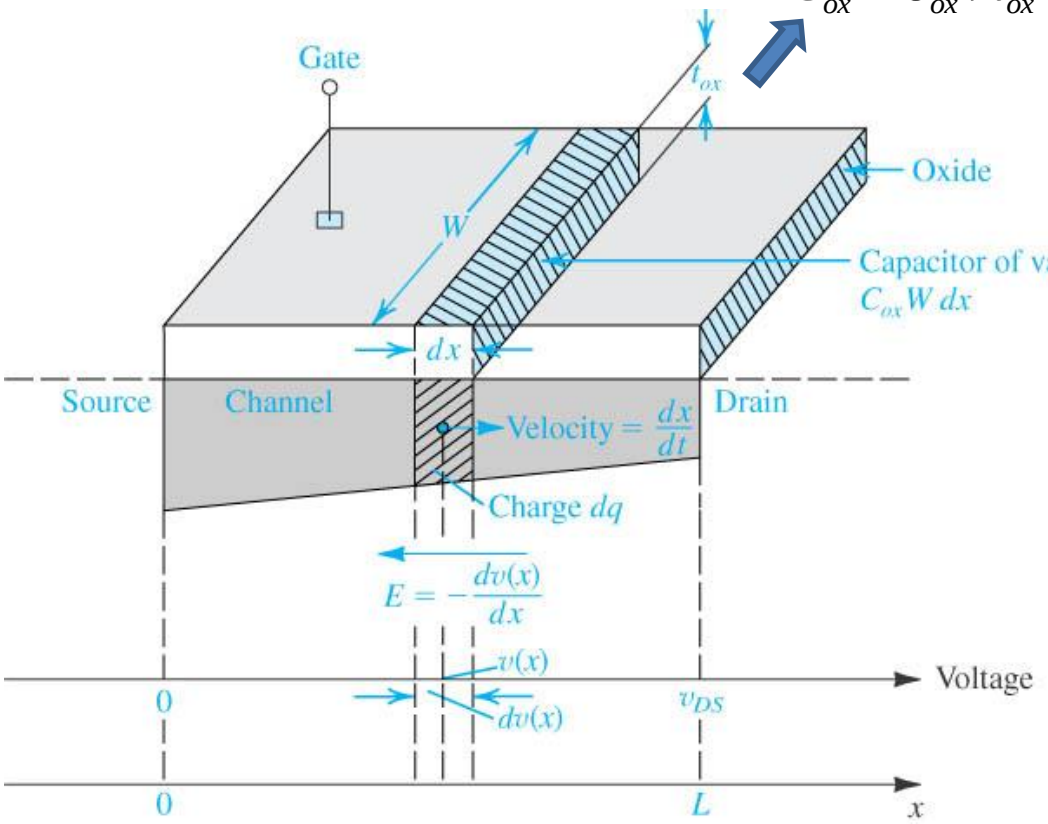
  $\Rightarrow$ called the saturation region





NMOS device structure

Derivation of i_D-v_{DS}



$$C_{ox} = \varepsilon_{ox} / t_{ox}$$

Strip dx: $C = C_{ox} W dx$

$$dq = -C\left(v_{GS} - V_T - v(x)\right)$$

$$\Leftrightarrow dq = -C_{ox} W \left(v_{GS} - V_T - v(x)\right) dx$$

$$E(x) = -\frac{dv(x)}{dx}$$

$$v_{drift} = \frac{dx}{dt} = -\mu_n E(x)$$

$$\frac{dx}{dt} = \mu_n \frac{dv(x)}{dx}$$

NMOS device structure

Derivation of i_D-v_{DS} (cont'd)

$$\frac{dq}{dx} = -C_{ox}W\left(v_{GS} - V_T - v(x)\right)$$

$$\frac{dx}{dt} = \mu_n \frac{dv(x)}{dx}$$

$$i = \frac{dq}{dt} = \frac{dq}{dx}\frac{dx}{dt}$$

$$i_D = -i = C_{ox}W\mu_n\left(v_{GS} - V_T - v(x)\right)\frac{dv(x)}{dx}$$

$$\Rightarrow \quad i_D dx = C_{ox}W\mu_n\left(v_{GS} - V_T - v(x)\right)dv(x)$$

$$\Rightarrow \quad \int_0^L i_D dx = \int_0^{v_{DS}} C_{ox}W\mu_n\left(v_{GS} - V_T - v(x)\right)dv(x)$$

$$\Rightarrow \quad \boxed{i_D = k_n' \frac{W}{L}\left[\left(v_{GS} - V_T\right)v_{DS} - \frac{1}{2}v_{DS}^2\right]}$$

with $k_n' = \mu_n C_{ox}$

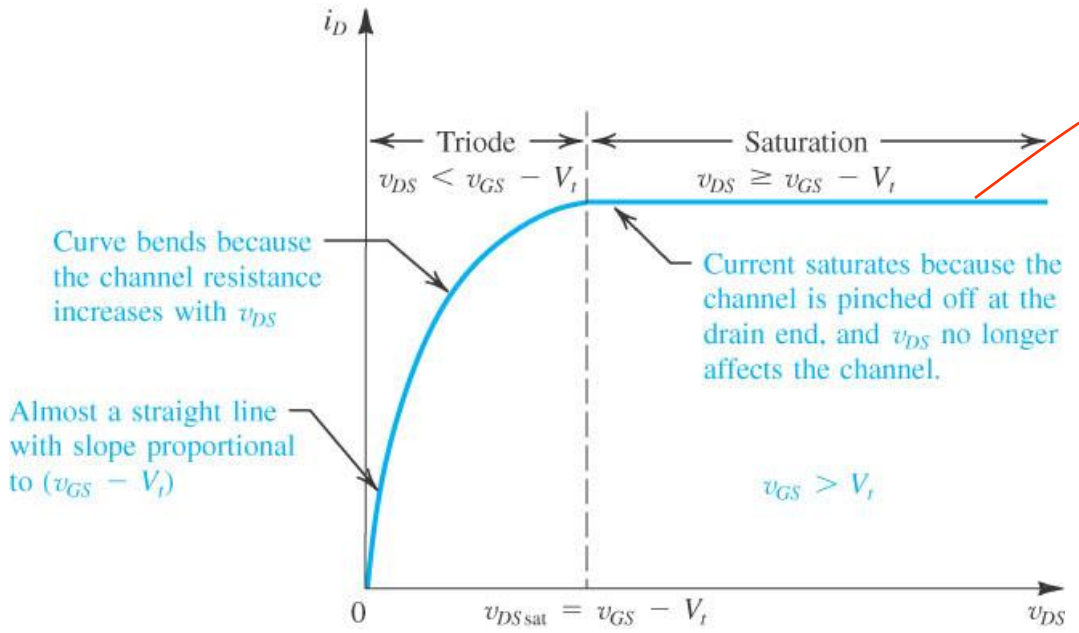
NMOS device structure

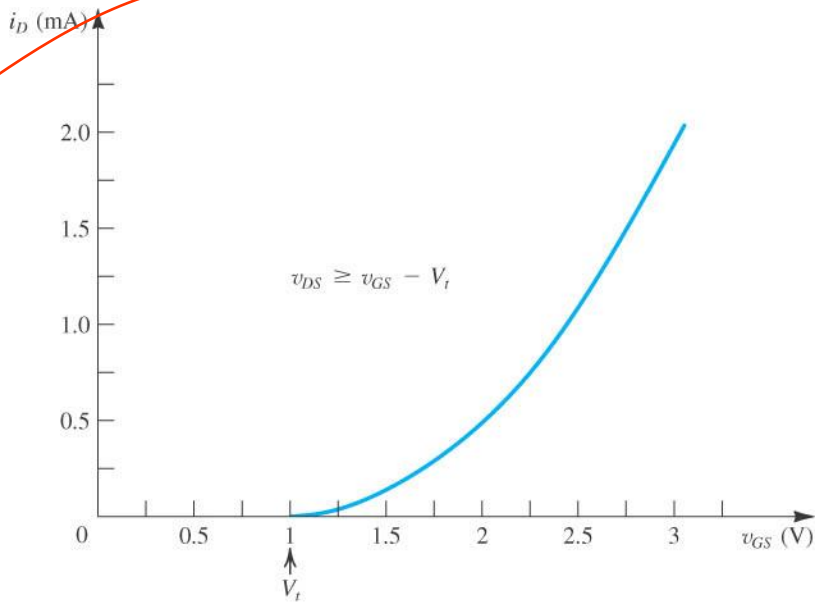
Derivation of i_D-v_{DS} : saturation region

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

saturation: $v_{DS} = v_{GS} - V_T$

$$\Rightarrow \quad i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_T)^2$$



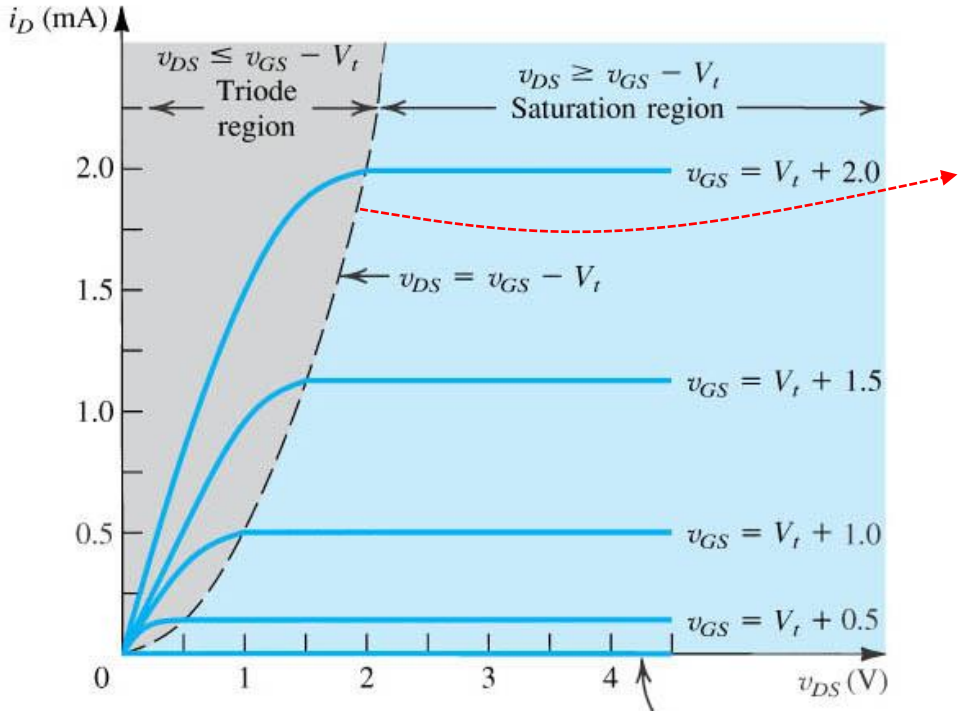


NMOS device structure

i_D-v_{DS} : summary

Triode region: $$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

Saturation region: $$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_T)^2$$



Limit between triode and saturation region:

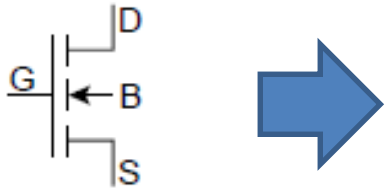
$$v_{DS} = v_{GS} - V_T$$

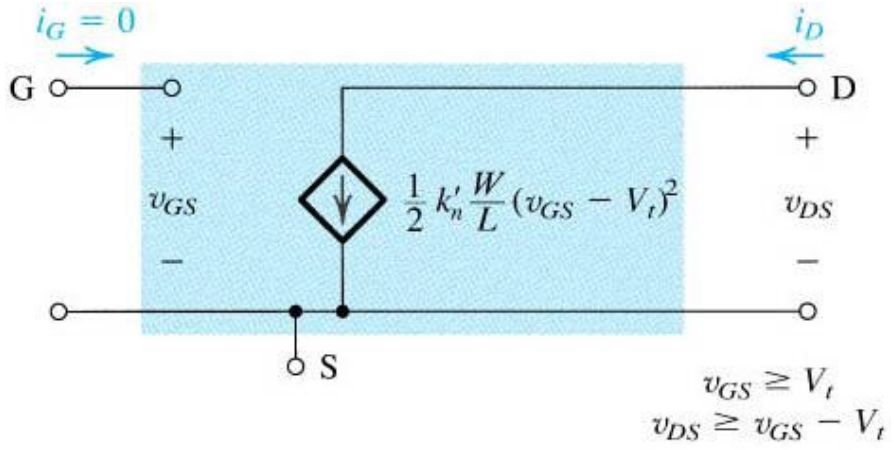
$$\Leftrightarrow i_D = \frac{1}{2}k_n' \frac{W}{L}v_{DS}^2$$

NMOS device structure

In saturation region…

- large-scale equivalent circuit
  - NMOS operates as a perfect current source
  - Input on gate: very high (infinite) input impedance
  - Valid for $v_{DS} \geq v_{GS} - V_T$

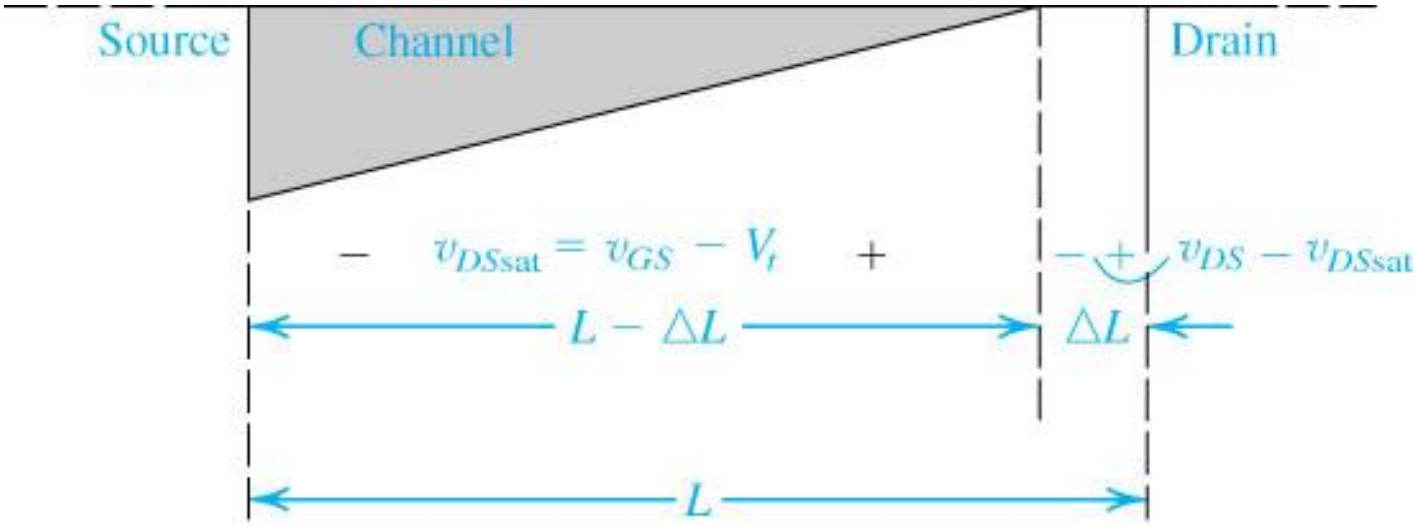




NMOS device structure

Saturation region: effect of channel pinching

- Increasing v_{DS} reduces the channel length
  - Voltage accross actual channel remains $v_{GS} - V_T = v_{DSsat}$
  - Electrons are accelerated through depletion region by additional voltage drop



NMOS device structure

Saturation region: effect of channel pinching

- Quantitative analysis:

$$i_D = \frac{1}{2}k_n' \frac{W}{L-\Delta L}\left(v_{GS}-V_T\right)^2$$

$$= \frac{1}{2}k_n' \frac{W}{L}\frac{1}{1-\left(\Delta L/L\right)}\left(v_{GS}-V_T\right)^2$$

$$= \frac{1}{2}k_n' \frac{W}{L}\left(1+\frac{\Delta L}{L}\right)\left(v_{GS}-V_T\right)^2$$

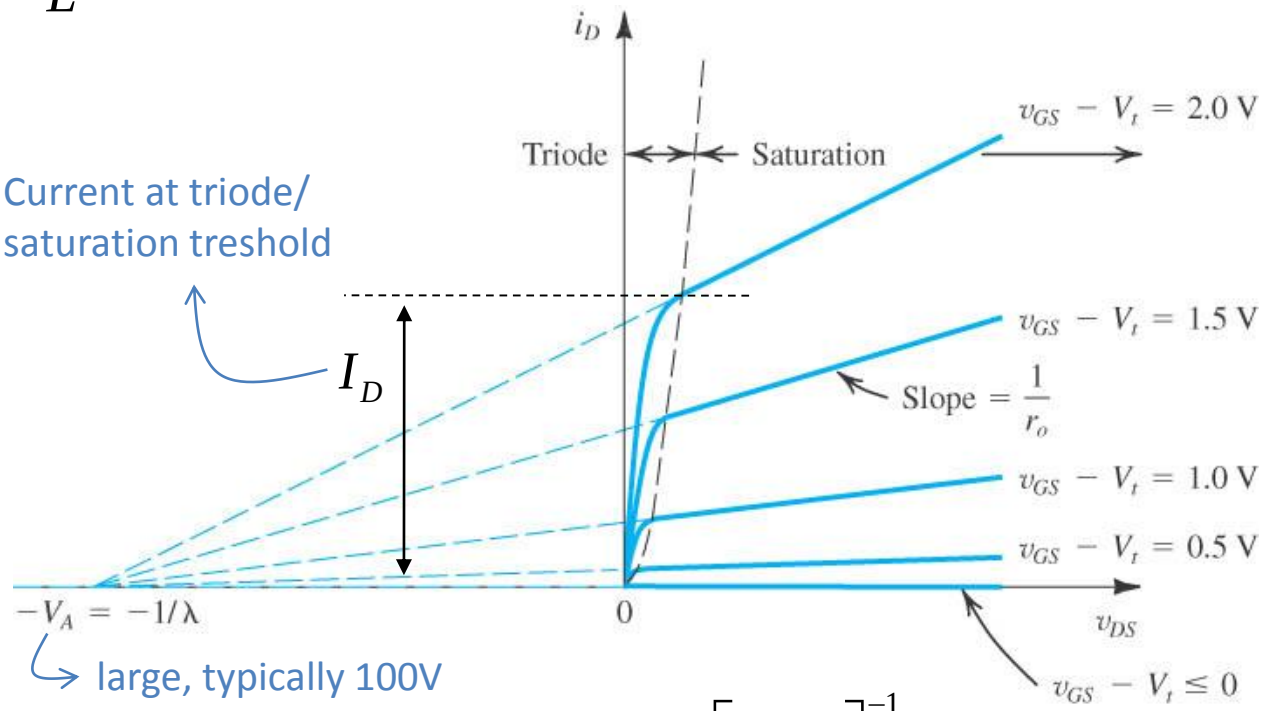
- Let us assume: $\frac{\Delta L}{L} = \frac{\lambda'}{L}v_{DS} = \lambda v_{DS}$

$$\Rightarrow \boxed{i_D = \frac{1}{2}k_n' \frac{W}{L}\left(v_{GS}-V_T\right)^2\left(1+\lambda v_{DS}\right)}$$

NMOS device structure

Saturation region: effect of channel pinching

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_T)^2 (1 + \lambda v_{DS})$$



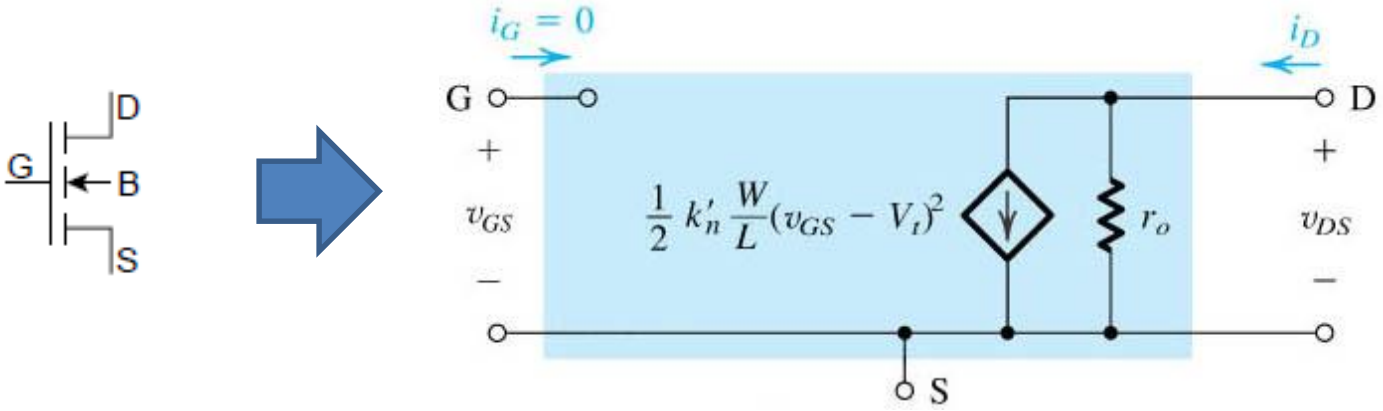
=> Output impedance of current source: $r_o = \left[\frac{di_D}{dv_{DS}} \right]^{-1} \approx \frac{1}{\lambda I_D} = \frac{V_A}{I_D}$

with $I_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_T)^2$

NMOS device structure

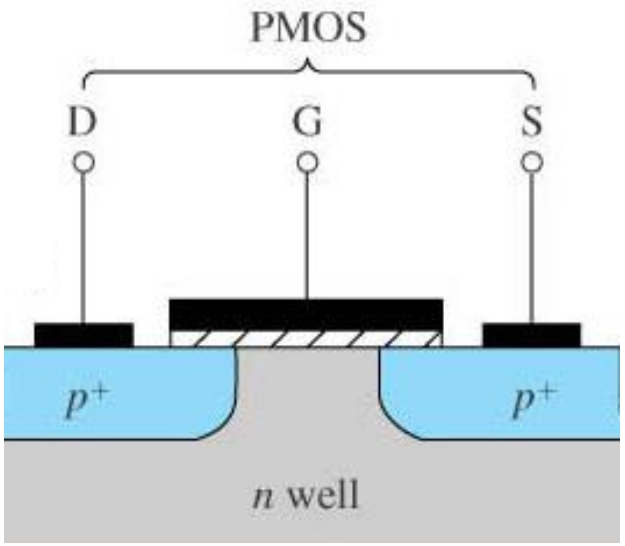
In saturation region…

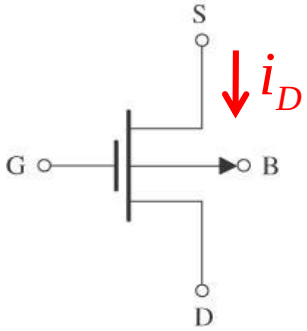
- large-scale equivalent circuit
  - Current source has output impedance r_o
  - Valid for $v_{DS} \geq v_{GS} - V_T$



PMOS transistors

… n-type substrate => p-type channel





(a)

Treshold voltage V_T is negative

$\Rightarrow$ v_{GS} needs to be « more » negative to create a channel: $v_{SG} \geq V_T \Rightarrow v_{GS} \leq -V_T$

$\Rightarrow$ Saturation when v_{DS} « more » negative than gate voltage: $v_{DS} \leq v_{GS} - V_T$

$\Rightarrow$ Current i_D (flowing **from source to drain**) in triode region:

$$i_D = k_n' \frac{W}{L}\left[(v_{GS} - V_T)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

$\Rightarrow$ Current i_D in saturation region:

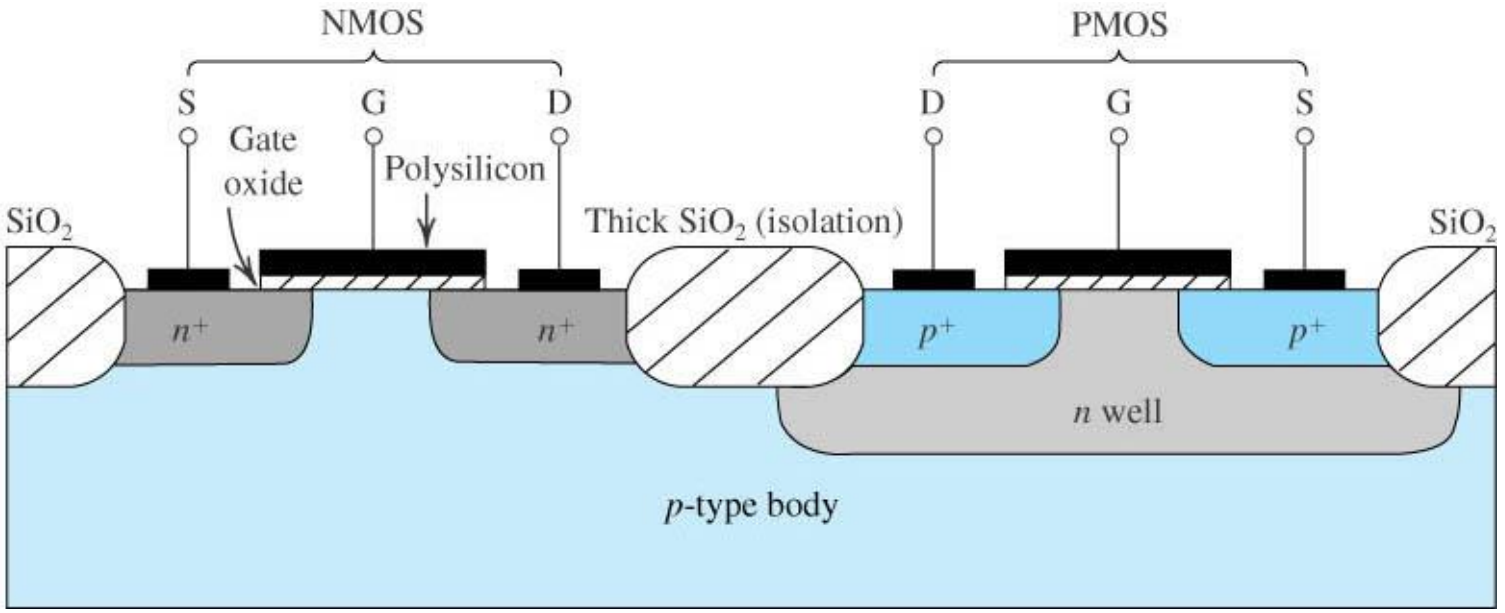
$$i_D = \frac{1}{2}k_p' \frac{W}{L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

Note that $k_p' = \mu_p C_{ox}$ and $\mu_p = 0.25\mu_n$ to $0.5\mu_n$

CMOS technology

Complementary MOS transistors

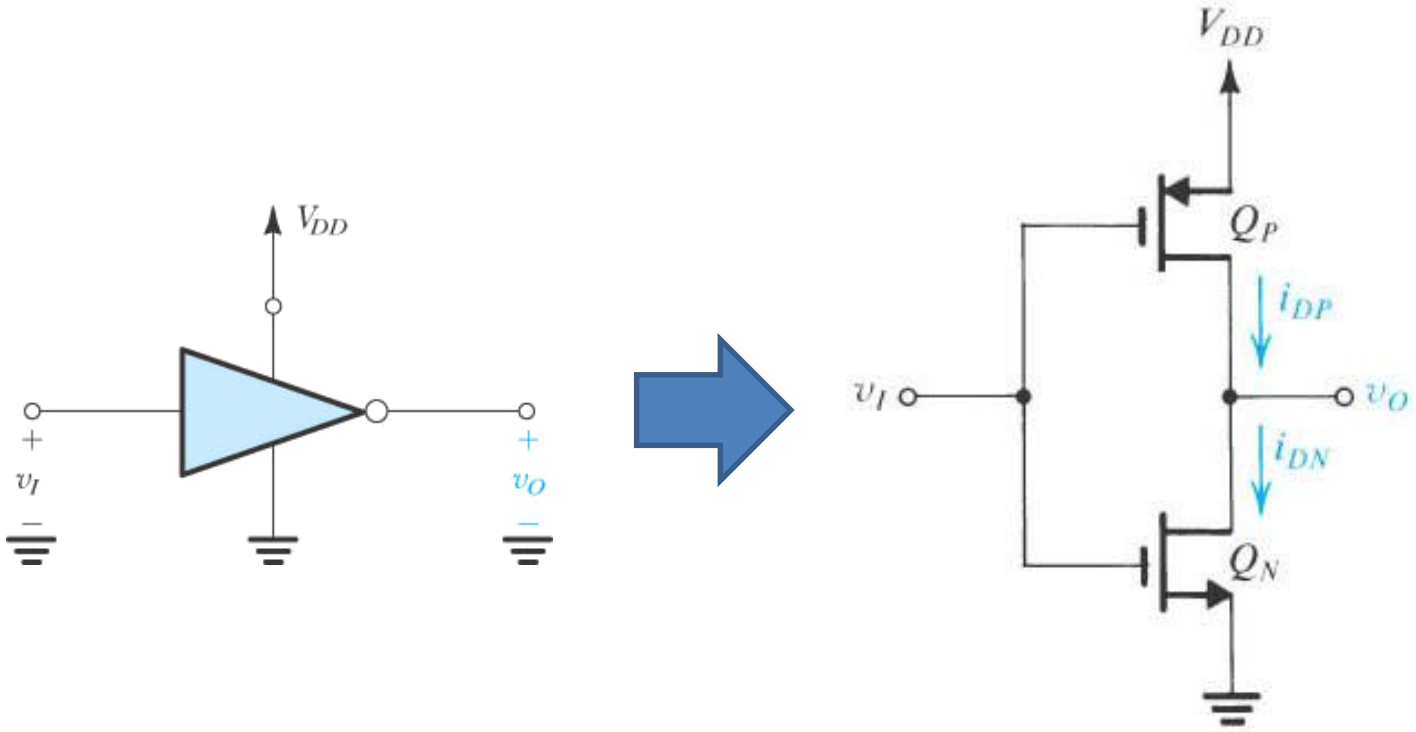
- Both NMOS and PMOS and same substrate
  - ⇒ Many powerful circuit-design possibilities
  - ⇒ Most widely used IC technology
  - ⇒ Many BJT applications now possible with CMOS



CMOS technology

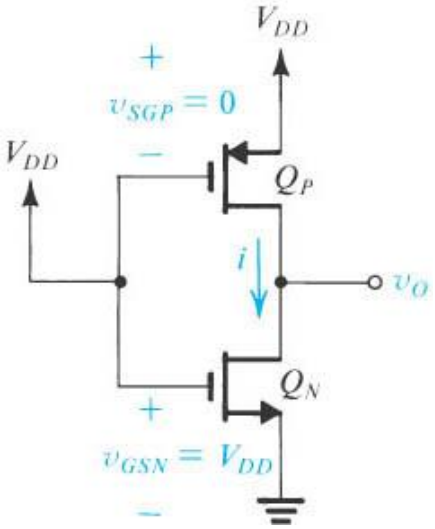
Example: CMOS digital logic inverter

- Digital logic inverter can be implemented with CMOS pair

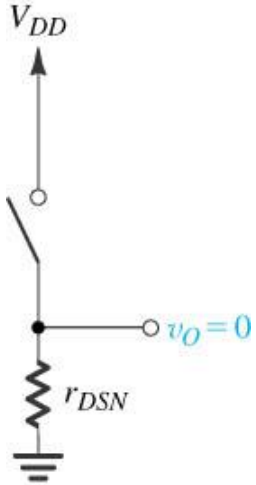


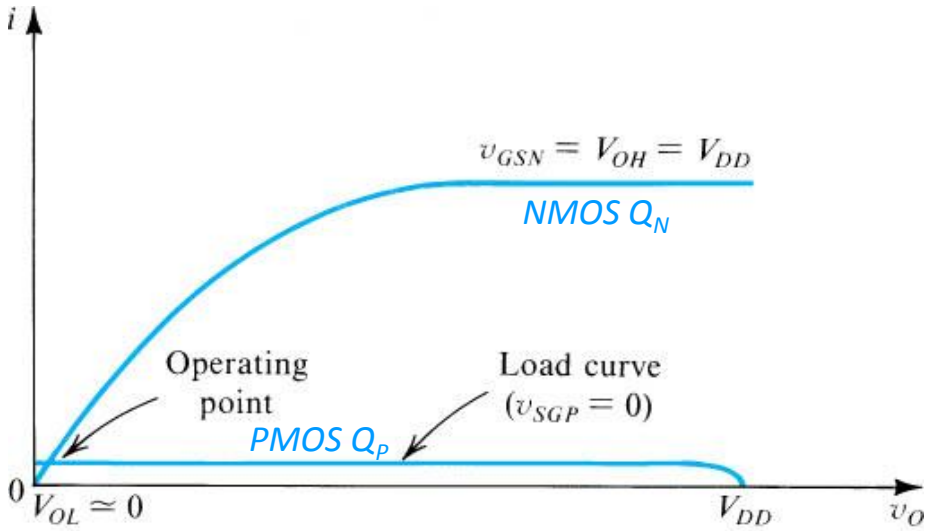
CMOS technology

Example: CMOS digital logic inverter (cont'd)



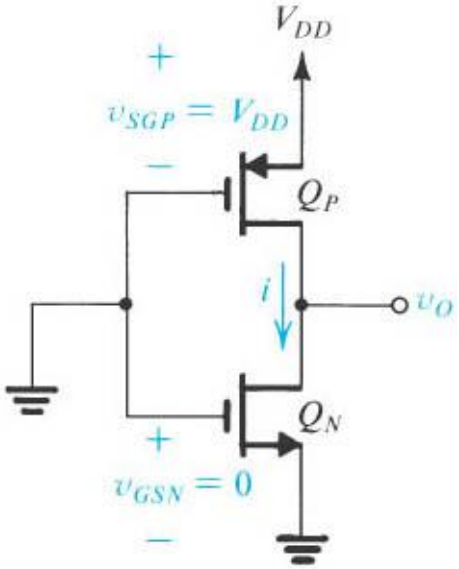
Input high
$\Rightarrow v_{GS}(Q_N)$ high, $V_{SG}(Q_P)$ low
$\Rightarrow Q_N$ passing, Q_P blocking
$\Rightarrow v_O = 0$



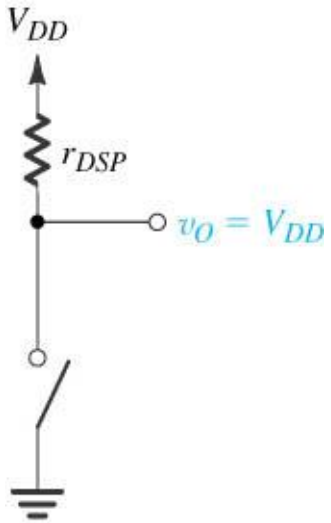


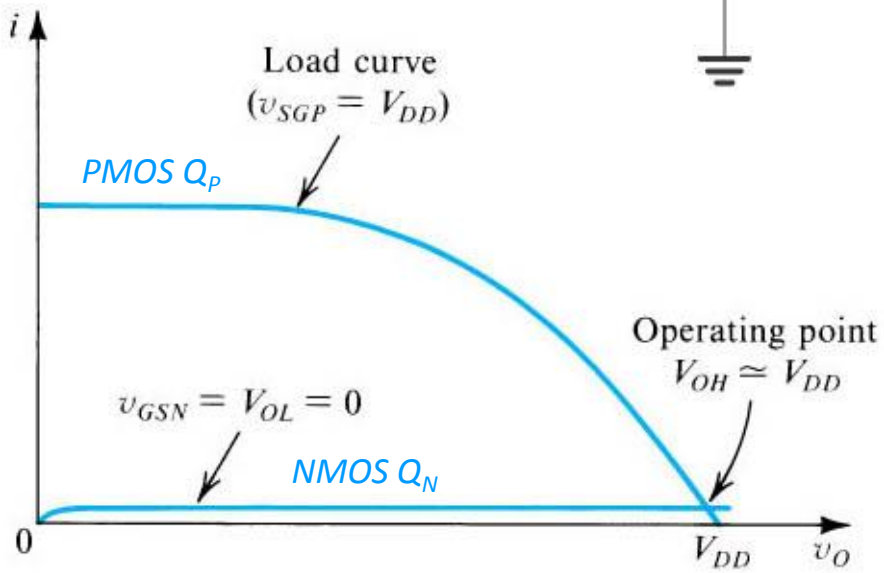
CMOS technology

Example: CMOS digital logic inverter (cont'd)



Input low
⇒ $v_{GS}(Q_N)$ low, $V_{SG}(Q_P)$ high
⇒ Q_N blocking, Q_P passing
⇒ $v_O = V_{DD}$





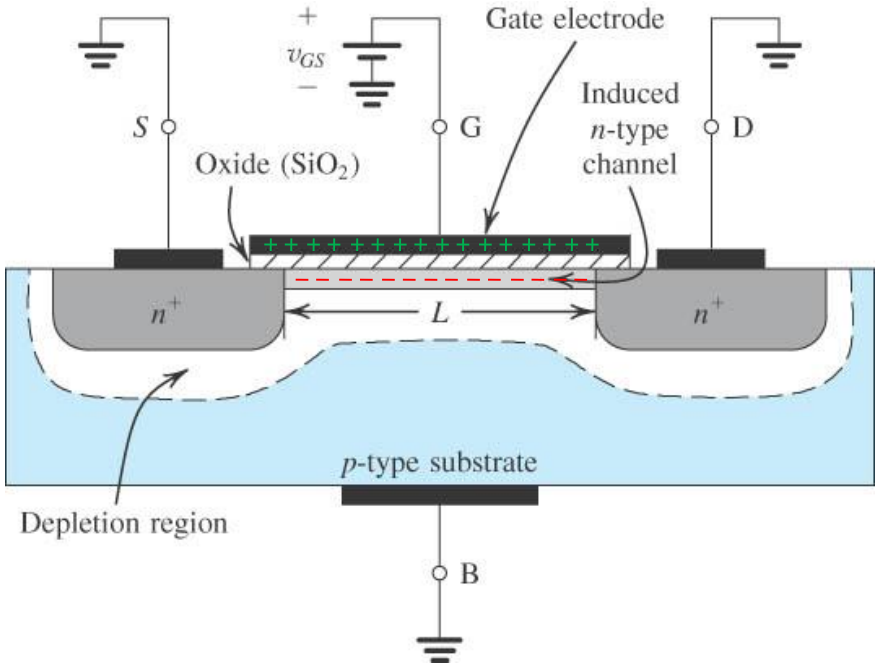
Effect of the substrate

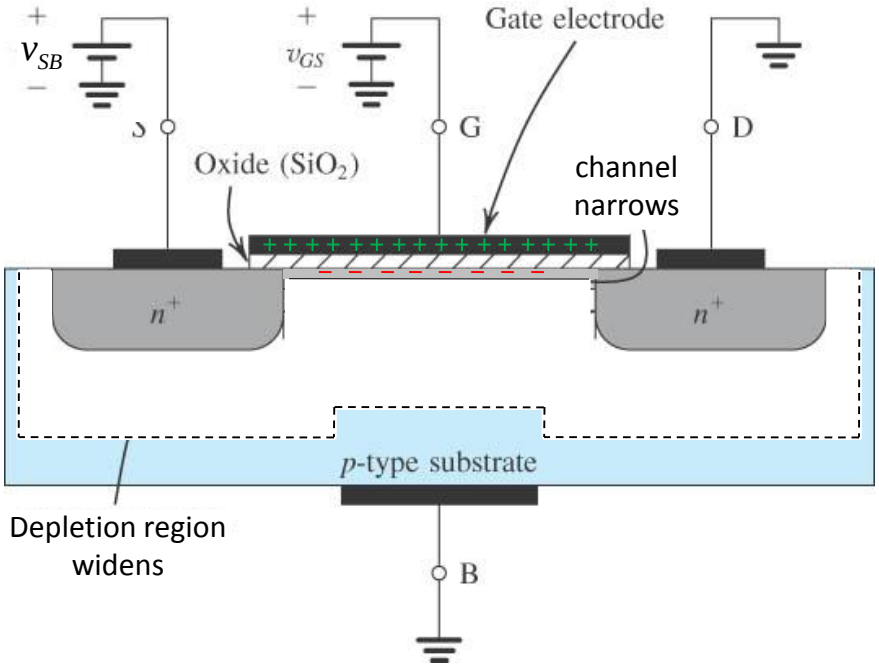
v_{SB} not alwas zero

- Substrate common to many MOS transistors

  $\Rightarrow$ usually connected to most negative power supply in NMOS circuit

  $\Rightarrow$ V_{SB} may not be zero for all transistors!





Effect of the substrate

V_t changes with V_{SB}

- Depletion region widens
  - $\Rightarrow$ More negative ions in depletion region
  - $\Rightarrow$ Less electrons required to compensate positive charges at gate
  - $\Rightarrow$ n-type channel narrows

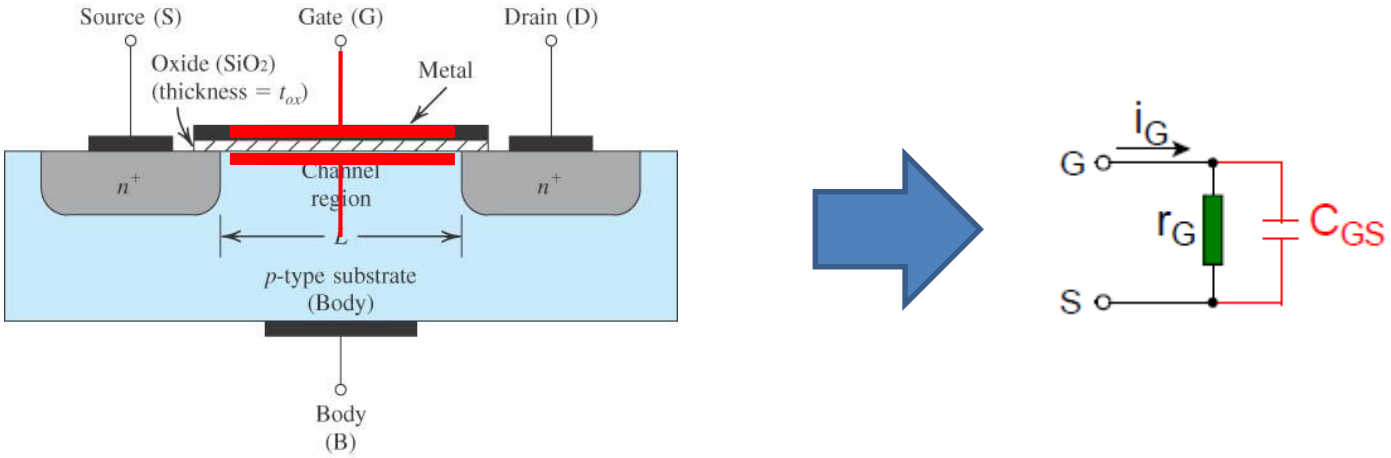
$\Rightarrow$ macroscopic effect: V_t increases

$$V_t = V_{t0} + \gamma\left[\sqrt{2\phi_f + V_{SB}} - \sqrt{2\phi_f}\right] \qquad \text{with } \gamma = \frac{\sqrt{2qN_A\varepsilon_S}}{C_{ox}}$$

physical parameter

NMOS input impedance

Gate acts as capacitor with substrate



- Input resistance r_G very high (~10^{15} Ω)
- C_{GS} ~ a few fF to some nF depending on size of NMOS

$\Rightarrow$ purpose of i_G is to load C_{GS}

$\Rightarrow$ static i_G is zero

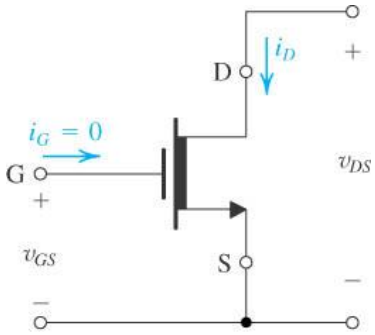
Depletion-type MOSFET

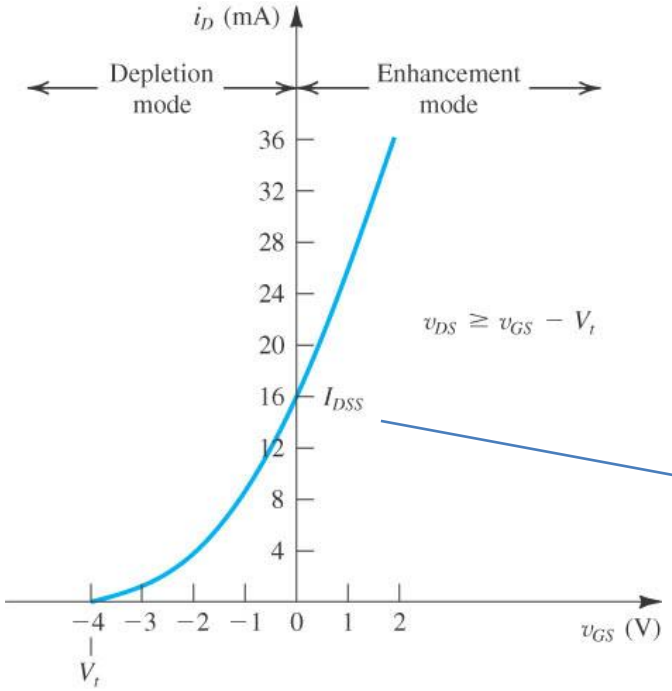
channel is physically implanted in MOSFET

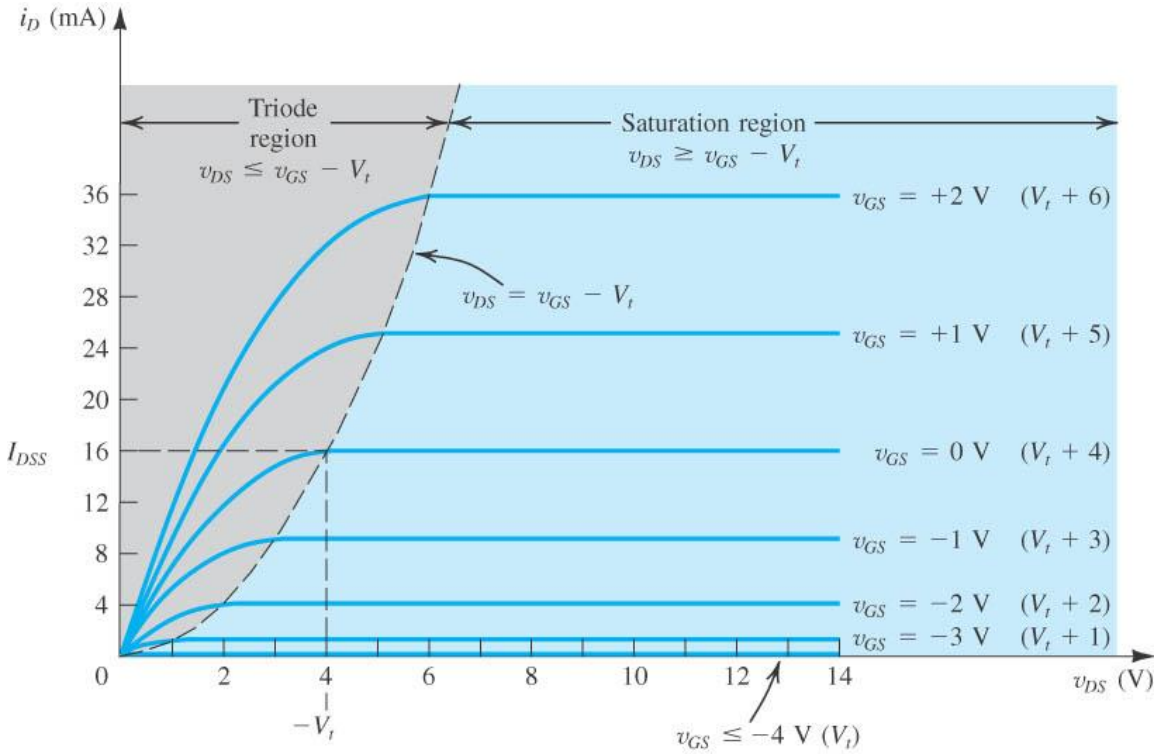
- For a NMOS, the channel is of type n
  - $\Rightarrow$ A n-type silicon region is implanted between the n^+ source and the n^+ drain at the top of the p-type substrate
  - $\Rightarrow$ If voltage v_{DS} is applied between drain and source, a current i_D flows, even for $v_{GS} = 0$
  - $\Rightarrow$ There is no need to induce a channel
- Channel depth and conductivity is controlled through v_{GS}
  - $\Rightarrow$ Positive v_{GS} : more electrons into channel => channel enhanced
  - $\Rightarrow$ Negative v_{GS} : electrons repelled from channel => channel becomes shallower => conductivity decreases

Depletion-type MOSFET

I-V characteristics







$$I_{DSS} = \frac{1}{2} k_n' \frac{W}{L} V_t^2$$

MOSFET characteristics

Enhancement-type vs depletion-type

- Enhancement-type and depletion-type MOSFET can be realized onto the same IC chip

  $\Rightarrow$ Circuits with improved characteristics